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Design of a 48-1.8V GaN based Dual Active Bridge converter with Phi-2 Resonant gating

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Design of a 48-1.8V GaN based Dual Active Bridge converter with Phi-2 Resonant gating

by

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To my dear parents Koteswara Rao and Sarojini Devi,brother Teja, my supporting friends and Dr.Bhuvaneswari ma'am

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Design of a 48-1.8V GaN based Dual Active Bridge converter with Phi-2 Resonant gating

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The dual active bridge isolated dc-dc converter is the most widely chosen converter for high-power density bidirectional power flow applications with its inherent galvanic isolation and ease of realizing soft-switching capabilities[1]. Modern power electronics often have to sustain higher ranges of loads and especially for applications like Point of Load (POL) regulators and data-centre specific applications where the conversion ratio is very high and also the converter lives in light load conditions for a significant part of its lifetime. In such converters the light load efficiency improvements without effecting the full-load conditions, thereby improving the overall efficiency of the converter is critical. One key learning for a converter design is that it is crucial when learning about more advanced converter topologies to understand the science behind how it works and especially understanding the design trade-offs.

The proposed converter architecture proposed in this thesis illustrates a 48-1.8V single conversion with an input-series-output-parallel (ISOP) architecture. The attractive features of the converter are (a) light load efficiency improvements without

impacting the full-load efficiency, (b) single-switch resonant gating design for a full-bridge inverter (c) data driven design strategy for the converter topology.

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Chapter 1

Introduction

1.1 Motivation for Dual Active Bridge

In recent years, the use of high frequency (HF) transformers instead of the traditional low frequency transformers has received a lot of attention and is considered to be the next-generation power conversion. There are a various advantages of high frequency transformers such as (a) low volume (b) low cost (c) avoid current and voltage waveform distortion due to avoiding core saturation and hit core loss limits first at MHz (d) lower noise. With the global climatic changes, in order to reduce the dependence on the non-renewable resources, the demand for energy systems have to be used to compensate the source variations and an isolated bi-directional converter with higher power-density and high-frequency operation capability is generally preferred to control the power flow between the energy storage and the load.[1].

The main motivation for Dual Active Bridge (DAB) converter for consideration for the high frequency transformer power conversions is its high power and isolated bi-directional power flow capabilities in case of active load, unlike its counterparts the unidirectional converters - like flyback, half-bridge and push-pull unidirectional converters. A full-bridge DAB converter is preferred as the number of switches increases, given the rated voltage and currents are the same for all the switches, the power capacity increases. For example, the eight-switch DAB converter is double the power capability of a four-switch converter as stated in [1]. Therefore for the 48-1.8V topology to maximize the power output and to make use of the transformer's voltage conversion- the galvanic isolated DAB converter is selected for this application. For this 48-1.8V applications include data centres power distribution, point-of-load (POL) converters connected to the 48V bus. Therefore to achieve high efficiencies with low cost and size, HF transformers-based topologies have been popular choice and thus DAB which also has an additional ease to achieve soft-switching in all the switches is chosen.[3].

Although DAB converters were first proposed in early 1990s in [4] due to the limitations of power devices and the reliability issues, it had limited applications. But the recent breakthroughs in processing GaN FETs (Gallium nitride power field-

effect transistors) with lower on-resistances (Ron), faster switching speeds and superior thermal characteristics compared with silicon power MOSFETs has made this topology more in demand in the recent decade. [5],[6],[7].

1.2 Thesis Outline

Chapter one covers the introduction to the thesis with the motivation and objective of the research. Chapter 2 is focused on detailed analysis of the DAB converter, its circuit configuration, steady state operations, switching commutations, converter architecture. It further also discusses the control methods and zero voltage switching (ZVS) analysis. Chapter two discusses the design procedure of the converter, detailed analysis and the trade-off analysis required to design the parameters of the converter. Detail discussion on the circuit configuration, steady state analysis of the converter and deadtime effects is covered in this chapter. The frequency of the converter selection, primary and secondary switches design and the gate drivers selection is discussed here.

Chapter three brainstorms over the novel design of the light load efficiency improvements and justify how this doesn't impact the full-load efficiency as one of the paper's goals as stated. Chapter four explains the motivation behind a resonant gating design for the converter and the various resonant gating methods. Then we dwell into the design strategy and analysis of the gate driver implemented for this converter.

Chapter five explains in detail transformer design for the the isolated converter chosen and design and in general process to design a transformer is also dwelt upon. Chapter six, we re-analyze the control methods that we introduced in the chapter two for the DAB converter control methods and discuss in detailed analysis of the state-space models of the control methods and the results.

Chapter seven is the experimental results and the analysis of the DAB converter designed. Chapter eight is a conclusion of the paper.

Chapter 2

Design of Dual Active Bridge Converter

This chapter discusses about the circuit configuration of DAB, different steady state operating conditions, commutation and then a detailed analysis of the design of the proposed 48V-1.8V, 100W DAB converter. This chapter is organized as follows: section 2.1 describes the circuit configuration and different operating modes of DAB converter. Section 2.2 then goes into the detailed analysis and derivation of the steady state input-output relations of the DAB and the soft-switching conditions and the ease of Zero-Voltage-Switching (ZVS) in a DAB converter is stressed upon. Section 2.3 to 2.7 dwell upon the design methodology and design parameters selection, the frequency, primary switch and secondary switch selection. Finally the gate driver design and isolator selection for the gate drivers and the supply voltages for gate drivers is discussed.

2.1 Circuit configuration

A DAB converter comprises of two H-bridges with four high-frequency controllable switches, a High-frequency transformer link conversion which provides galvanic isolation between the input and the outputs of the DAB. This has been in the past decade that we see the low-frequency transformers being replaced by the Hi-frequency transformers due to the size, low cost and to avoid the voltage and current distortions caused by the core saturation of the low frequency transformer. The key element of the DAB is the High-frequency transformer and the inductor which is the main energy transfer element in series with the primary of the transformer. This inductance could also be combined with the transformer as the leakage inductance in its primary and secondary windings. Especially high-frequency transformers have some amount of leakage inductance which will help reduce the load on the additional energy transfer inductance which needs to be included. Thus this main inductor's role other than acting as the energy storage/transfer element is to help with the soft-switching and thus reduce losses and improve the overall efficiency. Comprehensive analysis of the DAB converter in steady state is discussed in [8], [9] and [10].

Figure 2.1 shown below is the schematic of the traditional DAB converter with the two H-bridges and the main inductor and the High-frequency transformer. The inductor current controls the direction and magnitude of power flow to the load. The unique feature of the DAB converter is that unlike the traditional ac power systems which have line-frequency sinusoidal waves as voltages in both sides of the inductor the DAB converter has high-frequency square waves. This could be the case with other isolated topologies as well, but unlike other isolated topologies like flyback, LLC, etc., DAB the allows high-frequency at very high efficiency levels due to its ease of soft-switching on all switches. However this configuration shown can only block positive voltage and this is only for dc-dc power conversion. The control

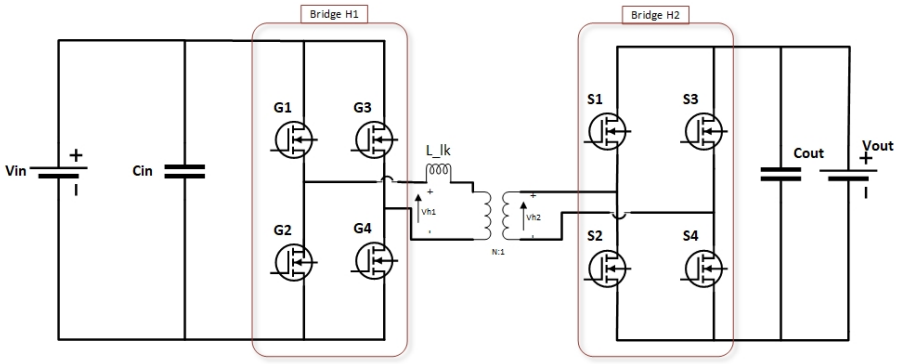


Figure 2.1: Schematic of the traditional DAB converter

scheme of the DAB converter is also not the traditional pulse width modulation (PWM), but it is controlled by phase-shift modulation (PSM) control strategies. All the switches in the DAB converter are operated at fixed duty cycle of 50%. The phase shift between the ac output square wave voltages v_{h1} and v_{h2} of the bridges H1 and H2 control the direction of power flow. Thus power flows from leading bridge to the lagging bridge.

2.2 Steady State Analysis

The basic form of the converter operates both full bridges at 50% duty ratio with a phase shift of ø between the vh_1 and vh_2. There are various phase shift strategies based upon the number of phase-shift angles is classified as single-phase-shift (SPS), dual-phase-shift (DPS), extended-phase-shift (EPS), triple-phase-shift

(TPS) [11], [12]. Although some papers have stated that EPS, DPS, or TPS can be used to improve the dynamic behaviour and efficiencies of the DAB, in the proposed DAB soft-switching techniques are applied and implemented to achieve better efficiencies and response times, thus considering real application and convenience of control, the SPS is the main control strategy. Thus considering SPS control strategy let us analyze and derive the input-output relations of the DAB. Consider the control pulses for G_1 through G_4 of the primary bridge and S_1 through S_4 of the secondary bridge with a phase shift of ø between the primary and secondary pulses thus having a positive power flow from primary to the secondary bridge. There could be three modes of operation: (1) $V_{in} = NV_{out}$, (2) $V_{in}<NV_{out}$ and (3) $V_{in}>NV_{out}$. Shown below 2.2 are the waveforms for the SPS control strategy.

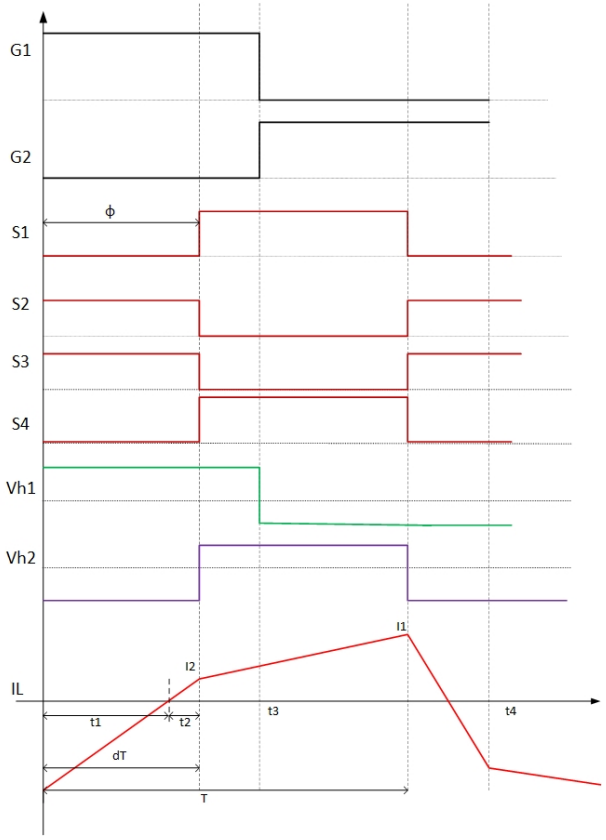


Figure 2.2: Waveforms of the DAB converter with SPS control scheme

So the DAB model can be analyzed as the the current waveform i_{Lk} through

the leakage inductance is expressed as [13]:

$$\frac{di_{Lk}(t)}{dt} = \frac{V_{pri} - V_{sec}}{i_{Lk}} \tag{2.1}$$

The cycle is divided into two parts:

$$V_{in} + NV_{out} = L_k \frac{I_1 + I_2}{dt} \quad 0 < t < dT \tag{2.2}$$

$$V_{in} - NV_{out} = L_k \frac{I_1 - I_2}{dt} \quad dT < t < T \tag{2.3}$$

$$\frac{I_1}{t1} = \frac{I_2}{t2} \tag{2.4}$$

$$\tag{2.5}$$

$$t_1 + t_2 = dt = \emptyset \tag{2.6}$$

Generally, solving these set of equations gives us:

$$I_1 = \frac{T}{2L_k}[2NV_{out}\phi + V_{in} - NV_{out}] \tag{2.7}$$

$$I_2 = \frac{T}{2L_k}[2NV_{in}\phi + V_{in} - NV_{out}] \tag{2.8}$$

Solving this with Matching mode, i.e, if $I_1 = I_2$:

$$< I_{out} >= \frac{\emptyset(1-\emptyset)TV_{in}N}{L_k} \tag{2.9}$$

$$< P_{out} >= \frac{\emptyset(1-\emptyset)TV_{in}V_{out}N}{L_k} \tag{2.10}$$

Therefore the relation between the input and the output voltage of the converter

can be obtained as:

$$M = \frac{< V_{out} >}{< V_{in} >} = \frac{\phi(1-\phi)TR_{load}}{L_k N^2} \tag{2.11}$$

where M = equivalent duty cycle ratio of dead-time in half switching cycle, D is the duty cycle of the switch, T is half-cycle switching period, N is the turns ratio, ø is the phase shift between the primary and the secondary [14].

2.2.1 Dead-Time Effects

The dead-time effect on the DAB converter are less comprehensively studied when compared to its control theories. Although dead-time has impressionable impact on the DAB converter operation, especially at high frequencies. The voltage distortion, efficiency degradation due to the voltage polarity reversal phenomenon and the phase drift phenomenon cannot be neglected.

A. Voltage polarity reversal

There is a voltage polarity reversal on the primary of the transformer due to the current flows reversely after the polarity of bridge H1 output voltage reverse, then the voltage returns to its original polarity. After this current flows through the diodes D_1 and D_4 instead of the two switches G_2 and G_3 during to the dead-time and this increases the back flow of the power and thus decreases the efficiency and also increases the stress on the switches. The power out remains constant as D increases in a certain range and begins to change approximately when the phase-shift is greater than the dead-time.

B. Voltage sag

Besides the condition described above there is a voltage sag that exists because of the coupled conductive diagonal switches in the low side of H-bridge and the same time there is no access for the current i_L in the high-voltage bridge. There could be some operation modes where we do not observe voltage polarity reversal or voltage sag but still the waveforms are not alike to those in traditional scheme. This can be attributed to the duty-cycle abnormality phenomenon. This could be either duty-cycle loss or duty-cycle addition.The duty-cycle abnormality is caused by large

leakage inductance. This causes because of the deadtime and thus secondary side duty-cycle loss. [15]

C. High frequency oscillation phenomenon

The voltage of the resonant inductor will be varied with the charging and discharging of the primary semiconductor junction capacitance, especially in non-matching mode as will be explained in the rest of the sections. When the phase-shift between the primary and secondary bridge is smaller than the relative phase-shift due to deadtime the secondary junction capacitor also participated in the oscillation together with the inductor and the primary junction capacitor during the deadtime period and lead to high frequency oscillations.

D. Phase drift Phenomenon

This phenomenon can be seen during deadtime which impacts the unified power output, the transmission power is less than zero and it remains constant as the phase shift increases in a certain range and then begins to change approximately when the phase-shift time is greater than the deadtime ratio. These can be seen significantly at the low power transmission applications. All these effects are non-ideal and are mostly not modelled into the power transmission analysis of the DAB converter and thus have to be careful to operate the converter in the best case mode as discussed below.

The dead-time effect can be analyzed in the three different modes of operation of the DAB converter.

(1) Matching mode:($V_{in} = NV_{out}$): In this mode we can say that the $i_L \geq 0$ and vt_2- $vt_1 \geq \mathrm{M}vT_{hs}$. Due to the perfect matching conditions, there are no polarity reversals and also the voltage sag is negligible in this mode. Thus in the proposed DAB converter the Matching mode is taken as the Best case scenario and also the average power remains independent of the equivalent duty cycle ratio of the dead-time.

$$< P_{out} >= \frac{\emptyset(1-\emptyset)TV_{in}V_{out}N}{L_k} \quad 2M \leq D \leq 1; M \leq \frac{D}{2} \tag{2.12}$$

where M = equivalent duty-cycle ratio of dead-time in half switching cycle and D is

the duty cycle of the switch

(2) $i_L \geq 0$ and vt_2- $vt_1 \leq$ M vT_{hs}: In this mode there is no voltage sag during vt_2- vt_3 but then here the output power delivered is dependent on M.

$$< P_{out} >= \frac{\phi(1-\phi)2TV_{in}V_{out}N(D-M)}{L_k} \quad M \leq D \leq 2M \tag{2.13}$$

2.3 Preliminary Design considerations

For the 48:1.8V conversion to have higher efficiencies at light load conditions without effecting the full-load behaviour needs high speed low power-loss devices with the best figure-of-merit. Also, for helping with soft-switching the architecture needs to be adjusted in order to help with this. The critical components of the DAB are the High frequency transformer design, the additional auxiliary inductance that is added to the traditional converter to achieve higher efficiencies and the Gallium Nitride Field Effect transistors (GaNFETs) and the DC blocking capacitors. The reasoning behind the architecture chosen, the frequency analysis will be outlined along with the key system parameters that are used for the component selection.

2.4 Converter Architecture

The 48:1.8 single converter has to be designed with the motive to have high efficiencies and also light-load improvements. Thus a Input-series-output-parallel(ISOP) architecture is chosen where the input 48V is divided into 2 series inputs thereby halving the rating requirement on the input capacitors and also the voltage conversion ratio. The second design strategy was to implement the primary of the DAB converter with a half-bridge instead of a full H-bridge so that would allow another halving of the voltage conversion ration and thus reduce the burden on the transformer turns ratio. The proposed converter architecture is shown in the Figure 2.3 below.

2.5 Primary bridge and frequency design

The half-bridge topology is designed for the primary bridge of the DAB converter as discussed above and the leakage inductance value is decided based

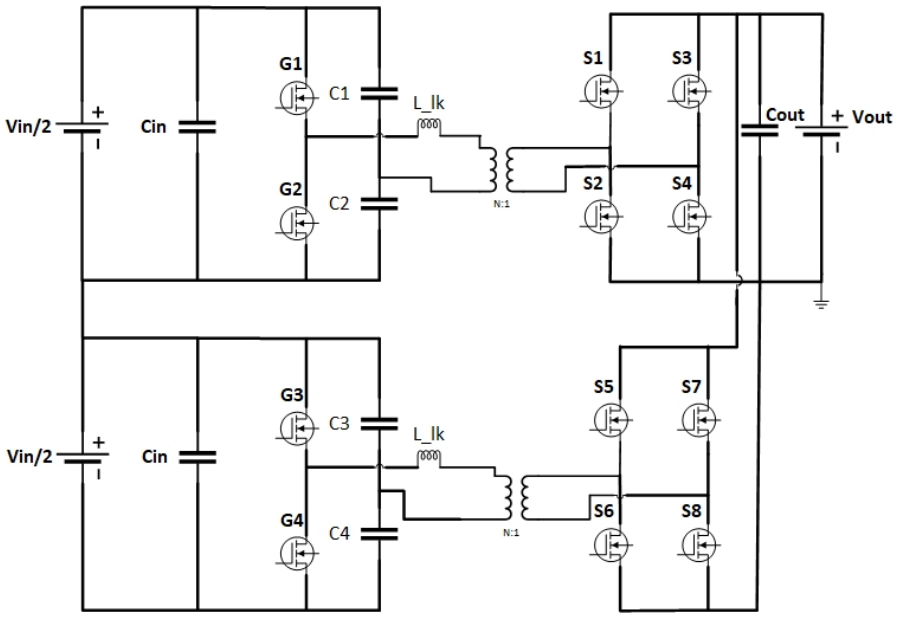


Figure 2.3: Proposed ISOP Schematic of the DAB converter

upon the power output decided for the converter, i.e., 100W. Therefore from the below equation 2.14 the leakage inductance needed for the converter is 103nH.

$$L_k = \frac{\phi(1-\phi)TV_{in}V_{out}N}{P_{out}} \tag{2.14}$$

The key parameters to be looked into to decide the optimal frequency of operation for the proposed converter are the dead-time and the conduction losses. As the dead-time is increased to lower the currents and thus reduce the conduction losses, the dead-time losses would surpass the incurred conduction losses, especially with GaN switches the body diode forward drop voltages are very high compared to MOSFETs. Thus analyzing these two constraints together gives us a range of acceptable On-resistance(R_{on}) of the primary switches. The results of the analysis shown in the Figure 2.4 below indicate that: With 1% hit in the efficiency we could have a good range of R_{on} at 3MHz switching frequency.

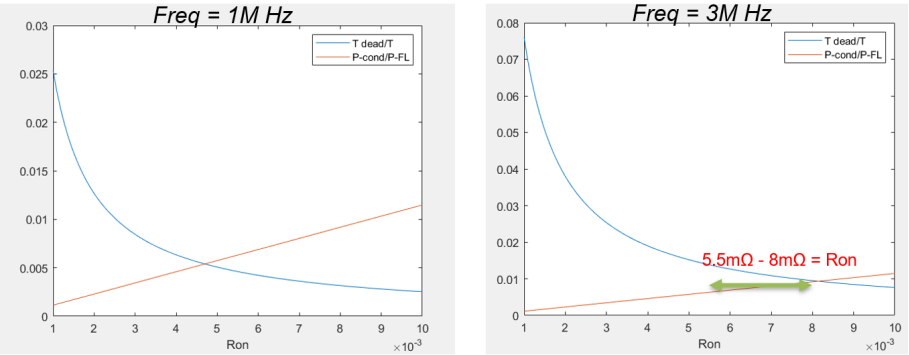


Figure 2.4: Frequency design analysis results

2.6 Zero Voltage Switching(ZVS)

The principle of Zero-voltage Switching(ZVS) which is soft-commutation of the switches is based upon the resonance between the inductance in the loop and the Drain-source capacitance, C_{oss} of the device during each switching cycle. The main motive to incorporate ZVS is to minimize losses and thus also could operate at much higher frequencies without incurring high penalties in switching losses. When the switch turns on/off with zero voltage/current respectively, then switching loss can be eliminated. ZVS can be achieved in various methods,the easier version without adding additional components to the design is with adjusting the dead-time of the devices. The basic principle is there should be enough energy in the inductor to completely discharge the capacitor and thus voltage on the switching node before turn on goes to zero thus ensuring ZVS turn-on for the switch. This is referred to as current commutation as well. The instantaneous current through the capacitance is given by:

$$I_{cs} = C_{oss}\frac{dV_{cs}}{dt} \tag{2.15}$$

$$I_{Lk} = 2 * C_{oss}\frac{dV_{cs}}{dt} \tag{2.16}$$

Thus, the total amount of energy stored in the inductor must be equal or greater than, the total energy required to fully charge/discharge the capacitors in order to

realize ZVS operation.

Now, considering the R_{on} achieved from the dead-time and the conduction loss analysis and to have higher Figure of Merit(FOM) we choose GS61008T, GaN systems part for the primary half-bridge.

2.7 Secondary switch Selection

In the secondary switch selection we need to analyze the total losses with several devices inorder to select the secondary switch with a data driven result. The drain-source voltages across the secondary switches is only 1.8V while the gate drivers are driven with 5-6V voltages based upon the MOSFETs and GaNFETs. To the first principles, the conventional gate-driving losses is equal to

$$P_{loss} = f_s V_g Q_g \tag{2.17}$$

where $f_s$is the switching frequency, V_g is the gate driver supply voltage, Q_g is the total charge of the MOSFETs. Thus the capacitance energy losses clearly show that the the gating losses are close to 10 times more than the switching losses. To reduce the gate driver losses there are several resonant gate drive techniques for the PWM converters. This is further discussed in the chapter 4. The device thus has only the high conduction losses, if we are able to achieve complete soft gating using the multi-resonant gate driver. Thus the main driving parameter in the selection of the secondary switch is the minimum drain-source resistance, $R_{ds,ON}$ along with the ability to operate at the switching frequency of 3MHz. Thus, looking at the available devices EPC2023 comes to be the best choice.

This could further be studied to improve the efficiency further by reducing the losses further, especially the conduction losses by having more devices in parallel for a single switch function. The losses division is analyzed in detailed as follows:

$$P_{cond} = 2 * {I_{rms}}^2 R_{on} \tag{2.18}$$

$$P_{sw} = 2 * C_{oss} {V_{out}}^2 f_{sw} \tag{2.19}$$

$$P_{softgating} = P_{reson} = P_{gdrv,M} + P_{cond,Rgd} + P_{ind} \tag{2.20}$$

where $P_{gdrv,M}$ is the gating loss of the switch in the resonant gate driver, $P_{cond,Rgd}$ is the conduction losses in the gate resistance and P_{ind} is the inductor ESL losses in the resonant tank. In the above equations, if we are analyzing for n switches in parallel: $R_{on}, n = R_{on}/n, C_{oss} = C_{oss} * n, C_{iss,M} = C_{iss,M} * n, R_{gd} = R_{gd}/n$

Analyzing these losses with varying number of switches in parallel with the EPC2023 gives the result figure 2.5 below:

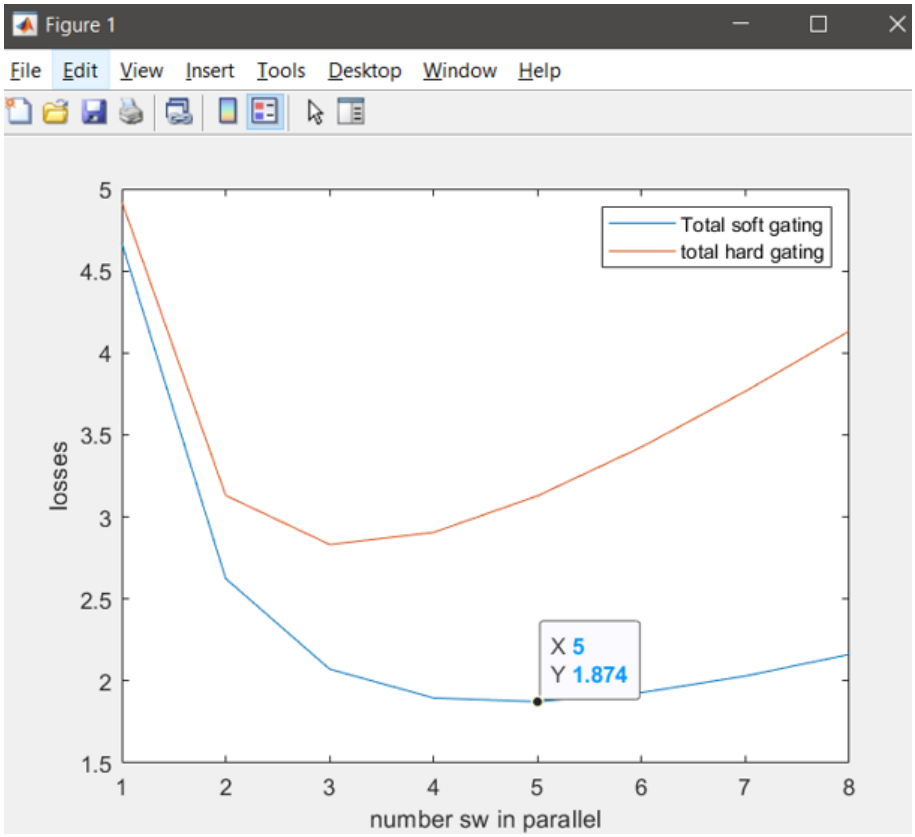


Figure 2.5: Secondary switch analysis in MATLAB

From the above figure 2.5 shows that we would require at least 5 EPC2023 GaN switches in parallel for each switching operation. This would make the board area and cost of the board very high. Going to a comparable Si MOSFET, among the devices available with lower R_{on}, TPWR6003PL, which has an $R_{on} = 0.55$ mΩ.

Using the equations 2.18 - 2.20 we can reanalyze the losses in the secondary and losses with 1 SiFET in parallel are comparable with 5 GaN switches in parallel. Thus we concluded to select the SiFET for the secondary switch instead of the GaNFETs.

2.8 Capacitor selection

The output capacitor of Dual Active Bridge is designed based upon the handling capacity of the ripple voltage. This value indirectly impacts the overall output voltage of the system, because it is the reservoir of the energy flowing to the output, and it also smoothes the output voltage. The key parameters in designing the output capacitor are: (1) Rated voltage (2) Rated ripple current (3) ESR (equivalent series resistance). The voltage and ripple current applied to a capacitor must be below the maximum ratings for the capacitor. The ESR is an important parameter that determines the output ripple voltage associated with the inductor current, and must be studied carefully.

The output ripple current is derived by writing KCL at the output node of the DAB converter:

$$I_{cap} = I_{HBridge2} - I_{load} \tag{2.21}$$

$$C\frac{dV_{out}}{dt} = \frac{V_{in}}{X_{Lk}}\Phi\left(1 - \frac{\Phi}{\pi}\right) - \frac{V_{out}}{R_{load}} \tag{2.22}$$

From the above equations 2.21-2.22 few inferences could also be made, such as the impact of the leakage inductance on the output capacitor, the higher the leakage inductance, larger output capacitor is required to maintain the ripple current. With these factors in mind output voltage ripple of 5% is chosen.

2.9 Primary Gate Driver

The Figure 2.6 below shows the block diagram of the gate driver circuit configuration. The MCP14700 is the main gate driver for the primary bridge for driving the GaN GS61008T switches of the power stage. The unique features to look for while selecting the gate driver for a GaN switches are the independent PWM

Input Control for High-Side and Low-Side Gate Drive so that dead time can be tightly controlled allowing for more efficient systems, low supply current.

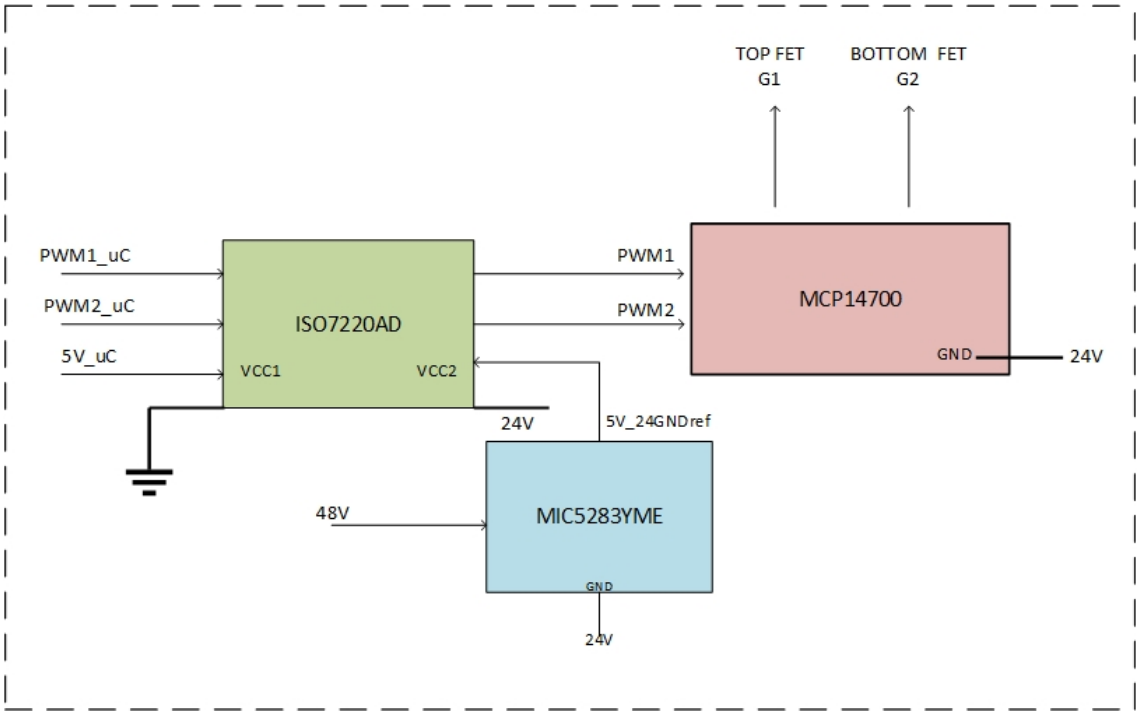


Figure 2.6: Gate driver configuration

2.10 Digital isolator

The primary gate driver for the top branch, which has a local ground of 24V, needs a level up from the ground reference. Thus is the requirement for the digital isolator, IS07220AD. This takes in the PWM signals from the micro-controller with one end at Vcc (5V) and ground reference and then isolated transfer the signals to the other end which is locally grounded at 24V, thus the output signals of the digital isolator are PWM signals for this top branch of the DAB converter, but the other end of the isolator needs a voltage Vcc2 of 5V which is referenced to 24V, this leads us to designing of linear regulators for the gate driver power supply as is discussed further in the section below.

2.11 Secondary Gate Driver circuit

Secondary gate driver design requires a resonant gate driver design as discussed in the section 2.7. The resonant gate driver topology proposed is the single switch Phi-2 resonant gate driver for the studied DAB converter and thus this is further discussed in detail in the chapter 4 along with the other resonant topologies. Also, from the chapter 4, we can see that the power supply for the phi-2 resonant gate driver is required to be 1.8V, which also needs to be generated from the 5V supply available.

The single switch of the secondary gate driver is also a GaN based switch as discussed in chapter 4, thus needs a low-side gate driver to drive this switch. LM5114, is selected to drive this GaNFET as this only requires a single switch gate driver, which has independent source and sink outputs to control the rise and fall times and also can withstand input voltages of upto 14V irrespective of the VDD supply.

2.12 Gate Driver bias power supply

As suggested in the above sections that we need several power supplies for the gate driver circuit. There are a total of 3 linear regulators required for the power voltages required. Given below is the list of the various linear regulators:

- Primary Gate driver: 48V Vin supply needs to be regulated to 5V, with a ground referenced to 24V.
- Secondary Gate driver: 5V micro-processor needs to be stepped down to 1.8V supply needed by the phi-2 resonant gate driver.
- 5V self generated, instead of pulling off of the micro-processor, this is an additional regulator to run the converter completely powered from the input voltage sourced itself. This would need 24V stepped down to 5V and regulated at 5V.

Inorder to meet all the voltage spec and requirements, MIC5283YME is chosen. This is a high performance adjustable output voltage linear regulator.

Chapter 3

Light load efficiency improvements

This Chapter discusses about the light load efficiency improvement techniques added to improve the overall efficiency of the converter. One of the main motives of the project is to achieve high efficiency over a wide range of load conditions and in doing so, making sure that the light load efficiency improvements do not effect or disturb the full-load conditions. This is required because in bidirectional dc-dc converters, especially with applications like computer power supplies, POL regulators the converter spends a significant amount of time in sleep state or low-power level states and also the input power oscillation can vary over a wide range and also the POL load could also vary a lot. In this particular application the load could also be zero in many cases, thus it is crucially required for the converter to be able to achieve high efficiency in a very wide range of loads.

In DAB converter, this is more significant because its light load efficiencies droop down very quickly as at light loads, the inherent nature of achieving Zero-voltage-switching(ZVS) of the converter switches, deteriorates. This is because ZVS is only maintained when there is enough energy stored in the leakage inductor to charge and discharge the switch parasitic capacitance during its deadtime. Unless, there is additional components that help "slosh" additional power back and forth across the capacitors to achieve ZVS as the load decreases. In order to achieve this study proposes a novel auxiliary inductance design in parallel to both the converters in the Input series output parallel(ISOP) topology. There have been various techniques that change the deadtime to improve the efficiency [16],[17],[18] of the switches and some add additional components to slosh power across the transformers leakage inductance, some require additional components for sensing[19].

This study explores the use of auxiliary inductance along with adaptive deadtime control, which will be explained in detail in the below sections, to improve the efficiency in DAB at light loads. This approach also ensures that we do not sacrifice or affect the high/full load efficiencies and thus improve the over efficiency of the DAB across all load conditions.

3.1 Circuit Configuration and Operation

The proposed circuit for light load efficiency improvements is shown in the figure 3.1 below with the 2 branches of the ISOP DAB converter, along with the auxiliary inductor in between them and a dc blocking capacitor. The auxiliary

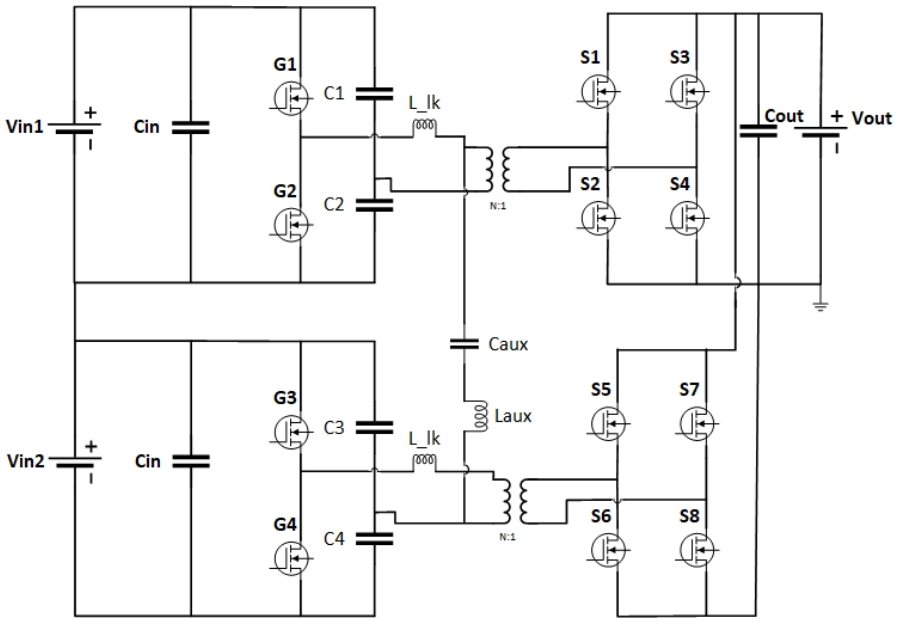


Figure 3.1: Light load efficiency improvements technique for DAB converter

inductor only is activated below a certain phase shift, or below a marked light load conditions. To start with the design, we would start with when there is no current in the main inductor what is the minimum required inductance in-order to achieve ZVS. From the ZVS equations we know that the current required for ZVS with C_{oss} of the switch and allowing a deadtime of T_{deadL}, we get:

$$I_{aux,pk} = \frac{2C_{oss}V_{in}}{T_{deadL}} \tag{3.1}$$

$$L_{aux} = \frac{V_{in}}{2I_{pk}}[(1-\phi)T_{hs} - T_{deadL}] \tag{3.2}$$

This would need to decide the deadtime in-order to achieve this ZVS. But we realize the trade-offs here in order to understand the optimum deadtime to achieve ZVS without much additional losses. Since these are GaN switches, the diode losses are very substantial and can be compared with the conduction losses. So analyzing the $\frac{P_{diode}}{P_{FL}}$ and $\frac{P_{cond}}{P_{sw}}$ is required to understand the trade-offs between both the losses and empirically arrive at a data driven decision. This analysis was done in MATLAB and the results shown in the figure 3.2 below indicate that there was just too much diode loss to have a fixed dead-time for this mode of operation. Thus concluding that adaptive deadtime is the optimal way of designing this auxiliary inductance control.

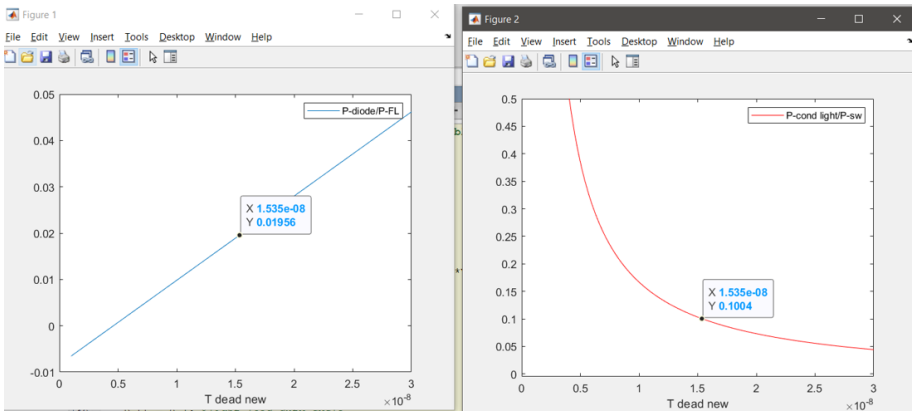


Figure 3.2: Fixed deadtime disadvantageous losses

3.2 Adaptive deadtime Control

In an effort to reduce the losses in the Dual active bridge converter, especially at high power and high frequency applications, there have been multiple techniques used as mentioned in the sections above, triangular and trapezoidal modulation to reduce the conduction losses in [20]. Then we moved on to the wide bandgap semiconductor devices to reduce the losses[21] and increase the switching frequency operation, reduce the voltage drops. Recently, there have been work with modifying the deadtime in order to achieve perfect ZVS and thereby reducing the losses. It has been studied that deadtime has a huge influence on the converter operation and commutation process and thus effects the overall losses of the converter. [22],[16].

Recollecting ZVS operation of the DAB, the ideal operation waveforms of the DAB are shown in the figure 3.3 below with Single Phase shift control and fixed duty cycle ratio of 50% for all the switches and a phase shift of ϕ between the primary and secondary H-bridges. As can be seen from the switching cycle that the switches G_1 and G_2 turn off at t_0 and t_3 and after the forward and the reverse deadtimes the switches S_1 and S_4 are turned on. This deadtime allows the inductor leakage current to slowly reduce to zero and thus allow switching at the zero crossing point, and allow soft switching and thereby reduce the losses. But to ensure this operation, the switches S_1 and S_4 must to turned on exactly at the zero crossing point, if the leakage inductance current crosses the ZVS point then there would be polarity reversal and the switch turns on at partial ZVS or hard-switching conditions. As can be understood from the equation 3.2 above, this deadtime is dependent on the leakage inductance, the input voltage and the switch parasitic, etc. Thus turning the switches On and Off has to be done at the exact instant otherwise there could be additional losses like reverse voltage and diode drops, especially with GaN devices these body diode losses could mean a huge hit in the voltage and thus the power delivered.

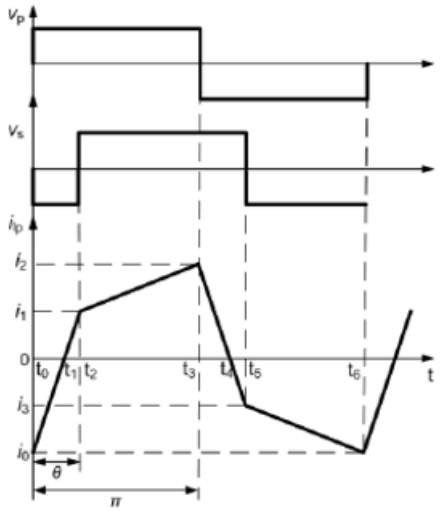


Figure 3.3: SPS controlled DAB converter voltage waveforms

With the advancement of the digital control, there are several new methods

of controlling the deadtime and the switching cycles inorder to improve the overall efficiency and adaptive deadtime control is an easy and straight forward answer to our problem, which was discussed in [16]. This scheme is a simple adaptive deadtime control for high frequency DAB converter. It feedbacks the drain-to-source voltage of the primary switches and accordingly tune the deadtime of the switches to make sure that primary switches are achieving complete ZVS at all operating conditions. But the issue is that the deadtime as described in the equation 3.2 is not as simple as it seems. This equation has greatly been simplified with a lot of assumptions for a starting point. The deadtime is actually a non-linear complex function of switch device characteristics, gate driver voltage, output current and also the temperature [17]. Therefore a fixed deadtime if chosen should be the longest possible deadtime required to achieve this, but increasing the deadtime will only make the losses to increase, especially with the diode losses after the voltage polarity reversal. According to [16] higher switching current require shorter deadtime and lower switching current require longer deadtime. This can also be interpreted as higher the current then shorter the time required to pull-off or put-on charge on the parasitic of the switch capacitors, thus needing shorter deadtime to achieve ZVS. But across switching currents, if we need to chose a fixed deadtime that would be the longest among all the switching currents which is to be chosen. But by doing so, fixed deadtime results in losing ZVS in some conditions and thereby increasing the switch stress, the losses and the overall performance of the DAB converter deteriorates.

Thus to mitigate this issue of ZVS loss with fixed deadtime issues, this study proposes an adaptive deadtime with the phase change which will be monitored from the drain-source voltage V_{ds} waveforms. The basic principle is to keep tracking the V_{ds} voltage and detect the voltage bump. If the V_{ds} bump is detected during the turn-on interval, then the deadtime should be decreased in the next switching cycle and vs-vs [16].

Chapter 4

Resonant gate driver design

This chapter discusses about the gate driver design and analysis of the secondary bridge. The motivation to design a resonant gate driver for the secondary switch is because of the topology 48V to 1.8V, 100W converter. The drain-source voltages across the secondary switches is only 1.8V while the gate drivers are driven with 8-10V voltages based upon the MOSFETs and GaNFETs. To the first principles, the conventional gate-driving losses is equal to

$$P_{loss} = f_s V_g Q_g \tag{4.1}$$

where $f_s$is the switching frequency, V_g is the gate driver supply voltage, Q_g is the total charge of the MOSFETs. Thus the capacitance energy losses clearly show that the the gating losses are close to 50 times more than the switching losses. To reduce the gate driver losses there are several resonant gate drive techniques for the PWM converters.[23],[24]. Thus the secondary gate driver is chosen to use a multi-resonant gate driver. The prevailing idea is to use a reactive component like inductor to behave like a current source to lossless charge and discharge the gate capacitance and thus enable soft-gating [25].The Reactive components, essentially store energy instead of dissipating energy and thereby the overall losses in conduction in any conventional gate driver circuit are eliminated. Moreover, if given a proper path, this stored energy in the reactive component can be pushed back to the power source, thereby ideally making it loseless.

In general, the C_{iss} of the GaN is much smaller than its counter MOS, SiC parts at the similar voltage and current ratings. Thus GaN can exhibit an order of magnitude reduction in the conduction and switching losses especially when operated at high frequencies. This is the main motivation to use Wide-bandgap (WBG) power devices in the resonant gate driver circuits and also are more viable choice for a gate drive circuit for WBG power devices based converters. Other advantages of Resonant converters over PWM are that the resonant converters are more sensitive to switching frequency, but less sensitive to the duty cycle perturbations and thus could handle the ZVS and zero $\frac{dv}{dt}$ conditions. But due to this dependence of

resonant converters on the switching frequency, most resonant converters, especially at high frequencies are self-oscillating.[26],[27]. Resonant gate drivers are made up of a passive phase-shift network of R-L-C components which could give a resonant output from the square-wave PWM signal, and thus resulting in soft-gating. This could be pure sinusoidal-resonant gate driver or a Quasi-square-wave $V_{gs}(t)$ [28].The sinusoidal resonant gate driver circuits are simple to design but lead to more losses than the quasi-square wave due to the slower rise and fall times during the switching causing more overlap in the $V_{gs}(t)$ and the $I_{gs}(t)$ leading to higher losses in conduction through the gate resistance R_g. On the other hand the quasi-square-wave resonant gate driver has a more trapezoidal based $V_{gs}(t)$ and thus faster rise and fall edges and thus leading to almost 90% reduction in the conduction losses in the gate driver.

Although the resonant gate driver circuit helps with loss reduction and thus improve the overall efficiency of the converter, there are certain drawbacks to this circuits, like these have a long start-up times. Due to this the bandwidth regulation of the converter is reduced and thus require more input and output capacitive filtering than the conventional gate drive circuit would need and also this design involves a very fine-tuning of the multi-resonant phase-shift network, which is very tedious and a repetitive process and thus complicated to implement.

4.1 Half-Bridge Resonant Gate Driver

Two gate driver topologies are proposed for the given DAB converter for the secondary side H-bridge MOSFETs. The first is shown in the figure 4.1 below, Half-Bridge multi-resonant gate driver also called as Juan-Rivas multi-resonant gate driver. This consists of a half-bridge consisting of S_a and S_b, and a multi-resonant network consisting of L_F, L_{MR} and C_{MR}.

The purpose of the multi-resonant network is to give an ideal quasi-sine-wave $V_{gs}(t)$ to the secondary switch. This is achieved by allowing only the first and the third harmonic components to pass through the network and reach the FET.The design principles as discussed in more detail in [25] when briefly stated are:

(1) To shape the $V_{gs}(t)$ in quasi-square wave across C_{iss}, the first and the third harmonic components should be in the ratio 3:1. Since the $V_{sw}(t)$ is already at duty cycle of 50%, when passing through the multi-resonant network, the gain

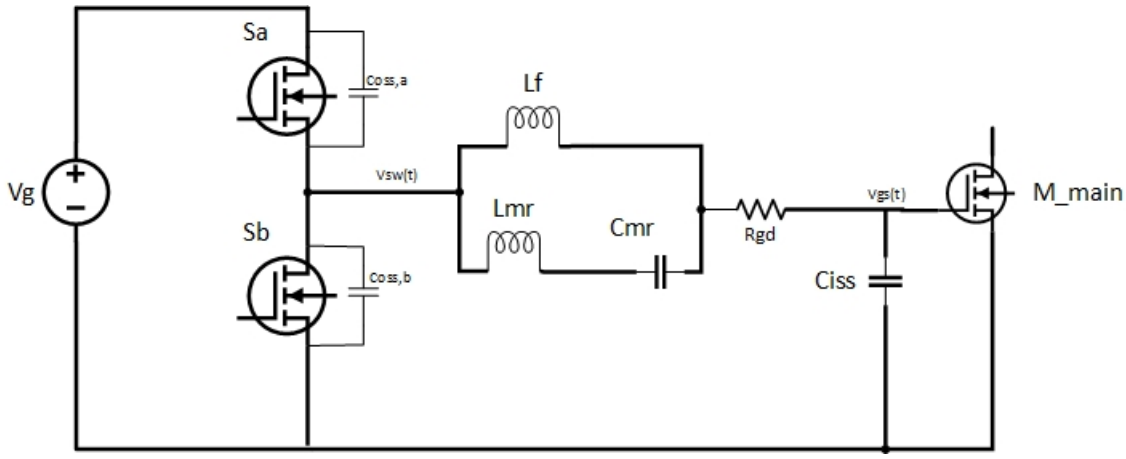


Figure 4.1: Half-Bridge Resonant gate driver

magnitude at f_{sw} and $3f_{sw}$ should be the same, as given below:

$$\left|\frac{V_{gs}(jw_s)}{V_{sw}(jw_s)}\right| \simeq \left|\frac{V_{gs}(j3w_s)}{V_{sw}(j3w_s)}\right| \tag{4.2}$$

(2) The phase shift at f_{sw} and $3f_{sw}$ should be the same and within the π to π range.The below are the equations governing this condition:

$$\phi_1 = \angle\frac{V_{gs}(jw_s)}{V_{sw}(jw_s)}, \phi_3 = \angle\frac{V_{gs}(j3w_s)}{V_{sw}(j3w_s)} \tag{4.3}$$

$$\phi_1 = \frac{\phi_3 + 2k\pi}{3}, k = 0, \pm 1 \tag{4.4}$$

(3) Gate drive FETs S_a and S_b must operate in ZVS to minimize any additional losses due to the multi-resonant network and thus the input impedance of the multi-resonant network must be inductive at f_{sw} and $3f_{sw}$ as shown in the figure 4.2 below and thus would give rise to the final condition to solve the three multi-resonant network parameters:

$$\Re(Z_{sw}(s)) = 0, \Im(Z_{sw}(s)) > 0 \tag{4.5}$$

From the above circuit analysis we get the below transfer function:

$$\left|\frac{V_{gs}(s)}{V_{sw}(s)}\right| = \left|\frac{1}{sC_{iss}Z_{sw}(s)}\right| \tag{4.6}$$

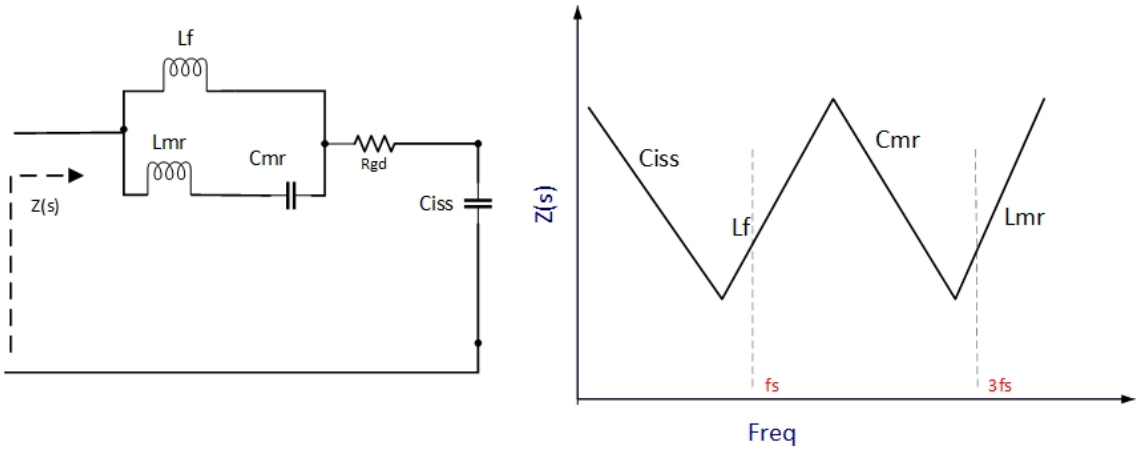


Figure 4.2: Impedance analysis off the resonant gate driver tan

Solving the above equations 4.2,4.4 and 4.5 we could solve the three multi-resonant network parameters. Another approach to solving this could be with the initial values of the three parameters: L_F, L_{MR} and C_{MR}. From the above bode plots 4.2 it can be seen that L_F and C_{iss} resonate at f_{sw} and L_{MR} and C_{MR} resonate close to $3f_{sw}$. Thus the starting values:

$$L_f = \frac{1}{(2\pi f_s)^2 C_{iss}} \tag{4.7}$$

$$L_{MR} = \frac{1}{(2\pi 3f_s)^2 C_{MR}} \tag{4.8}$$

Following the above mentioned principles the proposed multi-resonant gate driver is designed with the $L_F = 0.180\mu$H, $L_{MR} = 0.103\mu$H and $C_{MR} = 5.5$ nF. From the theoretical loss calculations, we could infer that the soft-gating losses were 38.5% lower than the hard-gating losses with the proposed gate driver circuit.

But the drawback with this resonant gate driver is that dead-time control of the secondary switch in order to achieve ZVS on the secondary H-bridge switches is

complicated and is not convenient to achieve complete ZVS on the secondary. This lead to the next research of the single-switch resonant gate drivers.

4.2 Single switch Resonant Gate driver

Single switch topologies are preferred for high-frequency due to low losses and more rigorous control. Single switch topologies allow deadtime control up to several nanoseconds range and also avoids the floating high-side (floating) transistor and therefore the synchronization issues between the high side and the low side devices and thereby simplifying the control methodology. Therefore, ground referenced low-side single-switch topologies are very attractive for high-frequency applications [29],[30].

Single switch topologies consist of a switch, inductor in series with input voltage and an LC resonant network. There are several variants of the single switch topologies but the two more prominent ones are the Class-E and Class-ϕ_2 gate driver topologies. These topologies allow ZVS with appropriate deadtime control and thus eliminate high switching losses[31]. One of the crucial conditions to be aware of while designing the single switch topologies is in order to keep the volt-second balance across the inductor which is in series with the input voltage, the average switch voltage has to be equal to the input voltage applied to the gate driver. However, the drawback of such topologies is the high-voltage stress on the switching device [32].

In class-E topology although has lot of benefits of an RF inverter but imposes a large voltage stress across the switch, almost close to 3.5 times the input voltage. This stress can be reduced using harmonic-tuned circuits using LC resonant network. But the large choke in this topology also slows down the transient responses. Thus this leads to more research on the class-ϕ_2 topology. This resonant network oscillates at second harmonic to switching frequency and is located in parallel to the switch, thus enabling a trapezoidal waveform across the switch. This trapezoidal waveform is the result of the first and the third harmonics combined as shown in the figure 4.3 below [31].

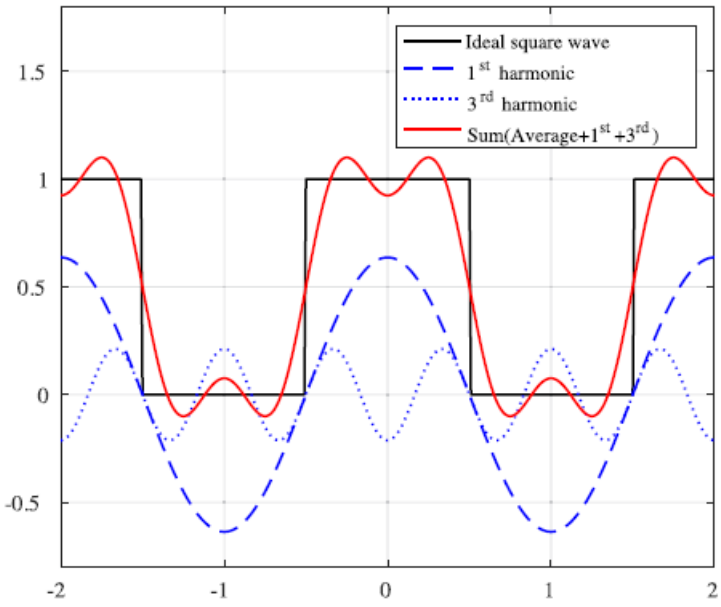


Figure 4.3: Addition of first and third harmonics to form quasi-square wave

4.3 Analysis of the Proposed Gate Driver topology

A single switch topology, Class-ϕ_2 is chosen as a result of the above advantages of this topology. Figure 4.4 below shows the schematic of the proposed single-switch Class-ϕ_2. It consists of DC voltage source V_g in series with an inductor L_f, a ground referenced switch M, passive network C_{MR},L_{MR}. This resonant network is connected in parallel to the power driven MOSFET M_{main}, which has a gate resistance of R_g and input capacitance C_{iss}. The ground referenced switch is driven at 50% duty cycle and satisfies ZVS. The series inductor L_f helps achieve the soft-gating by interacting with the C_{iss} of the main power switch and the C_{MR},L_{MR} resonate at 2^{nd} fundamental frequency in order to achieve more trapezoidal-like V_{gs} and thus improve the voltage stress on the gate drive FET, i.e, M and also reduce the switching losses in the main powerfet as the rise and fall times are faster in trapezoidal V_{gs}.

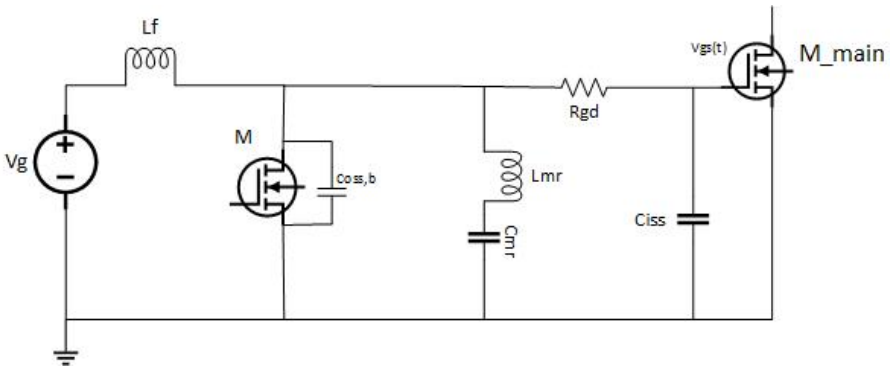


Figure 4.4: Proposed single-switch gate-driver circuit

4.3.1 Steady-state Analysis

The circuits with varying current and voltage responses based on the switching cycle are analyzed in piece-wise linear functions. Here the circuit behaviour is discussed in detail in each switching interval. When the switch M is turned on, it can be modelled as a resistor with a resistance of the drain-source value(R_{ds}) and during turn off R_{ds} can be ideally considered as infinite. Also the C_{oss} of the switch is taken into consideration for the turn-on and turn-off process.

Turn-ON - $DT \leq t \leq T$

The equivalent circuit during turn on stage is shown below in the figure 4.5:

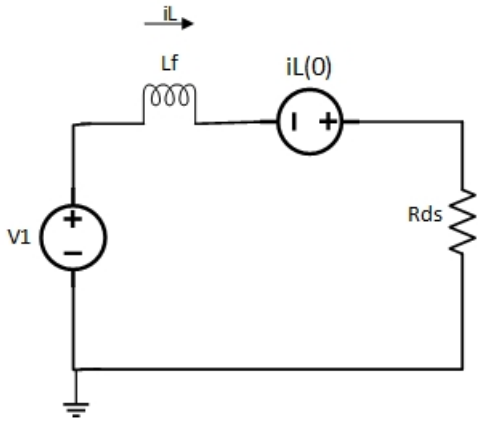


Figure 4.5: Equivalent circuit when switch M is closed

In this time interval, the switch acts as a resistor R_{ds} and since this drop is so low that the V_{gs} across the C_{iss} of power switch M_{main} is zero, leading to turn off the main power switch. In this time interval, i_g is zero and C_{iss} is discharged. Writing the KVL equations we could calculate the instantaneous inductor current i_L:

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L(t)dt + i_L(0) = \frac{V_1}{L}(t - DT) + i_L(0) \tag{4.9}$$

At end of this interval the inductor current is:

$$i_L = \frac{(1-D)V_1}{f_s L} + i_L(0) \tag{4.10}$$

Also, the switch current can be obtained from the below equation:

$$i_M = \frac{(D)V_1}{(1-D)L}(t - DT) - \frac{(1-D)V_1}{2f_s L} \tag{4.11}$$

Switch-Off - $0 \leq t \leq DT$

The equivalent circuit during this time interval is shown in the figure 4.6 below. During this interval the switch M is turned off. The switch voltage is equal to the V_{gs} of the main switch M_main. In order to obtain a trapezoidal V_{gs} we need to add the passive resonant components L_{mr}, C_{mr} in parallel to the switch M. The inductor L_{mr} and the capacitor C_{mr} are tuned to conduct at the second harmonic current component.

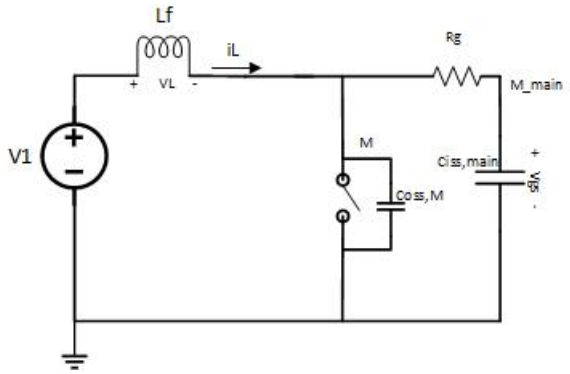


Figure 4.6: Equivalent circuit when switch M is opened

$$w_r = 2w_s = \frac{1}{\sqrt{L_{mr}C_{mr}}} \tag{4.12}$$

where w_s is the fundamental frequency. The current through the resonant network is sinusoidal waveform and can be expressed as:

$$i_m r(w_{mr}t) = I_m sin(2w_s t + \phi) \tag{4.13}$$

Where I_m and ϕ are peak amplitude and the phase of i_{mr}. From this we could obtain the inductor current.

$$i_m r = i_L + i_G \tag{4.14}$$

where i_G is the gate current which is given by:

$$i_G = C_{iss}\frac{dV_{Gs}}{dt} \tag{4.15}$$

Combining equations 4.13 and 4.15 and substituting in 4.14 gives:

$$C_{iss}\frac{dV_{Gs}}{dt} = \frac{1}{L}\int_0^t v_L(t)dt - I_m sin(2w_s t + \phi) \tag{4.16}$$

This can be simplified into second order non-homogeneous differential equation:

$$\frac{d^2V_{gs}}{dt^2} + \frac{V_{Gs}}{C_{iss}L} = \frac{V_1}{C_{iss}L} - \frac{2w_s t}{C_{iss}}I_m Cos(2w_s t + \phi) \tag{4.17}$$

The particular solution for this second-order equation is:

$$V_{Gs}(w_s(t) = V_1 + \frac{2a}{4a^2 - 1}Z_0 I_m cos(2(w_s t + \phi) \tag{4.18}$$

where

$$a = \frac{w_s}{w_0}, Z_0 = \sqrt{\frac{L}{C_{iss}}}, w_0 = \frac{1}{\sqrt{LC_{iss}}} \tag{4.19}$$

Here a is the frequency ratio, Z_0 is the impedance and w_0 is the resonant frequency. In order to produce the desired trapezoidal voltage V_{gs} consisting of only the 1^{st}

and the 3^{rd} harmonics the resonant frequency should be less than or equal to three times the fundamental frequency [33].

4.4 Design Principles

The proposed gate driver is designed at the switching frequency of 3MHz. In order to determine the parameters of the resonant gate driver L_{mr}, C_{mr}, L_f, we choose a 50% duty cycle for the switches for this purpose. Although, this is not the limit and could be designed for any other duty cycles. The secondary switch, power MOSFET selected is TPWR6003PL based upon the tradeoffs discussed in chapter2, section 2.7 This power MOSFET has a large C_{oss} of 2.72nF, C_{iss} of 7.7nF. The switch for the resonant gate driver is selected based on the best Figure of Merit(FOM) and having the lowest possible losses in the switching losses. Therefore, the GaNFET, GS61004B is selected for the switch M, which has a C_{oss} of 300pF. The impedance analyzer gives more details about the parameters value decision. The tuning of the component parameters should lead to the following results:

- The impedance should be inductive at the fundamental frequency, with a phase angle between 30 and 50°, this is to ensure that we achieve ZVS on the switch M. This makes sure that the zero-crossing point of the switch voltage is prior to the switch current and thereby reduce the losses in the switch M.

- In the second harmonic frequency, the magnitude of impedance is ideally null, but practically small due to the resonant network.This is to reduce the peak V_{ds} voltage of the switch M.

- The impedance is capacitive and high magnitude at frequency around and lower to third harmonic frequency.

With these principles in mind, tuning the C_{mr}, L_{mr} can be started such that the impedance maxima of the Z_{mr} are at the fundamental and the third harmonic frequencies. The initial value of C_{mr} is chosen based on the tuning the poles of impedance transfer function exactly at fundamental and the third harmonic and placing a zero at the second harmonic. This can also be interpreted as the C_{mr} and L_{mr} resonate with 2nd harmonic frequency to lower the peak voltage and shape

the trapezoidal voltage, while the C_{iss} of the power MOSFET M_{main} and the L_f resonate to get the resonant frequency w_o [34].

$$C_{mr} = \frac{15}{16} C_{oss} \tag{4.20}$$

This is C_{oss} of the switch M, in the proposed gate driver it is the GANFET GS61004B, which is 300 pF

$$L_{mr} = \frac{1}{C_{mr}} \left(\frac{1}{2 \times 2\pi f_s} \right)^2 \tag{4.21}$$

$$L_f = \frac{1}{C_{iss}} \left(\frac{1}{2\pi f_o} \right)^2 \tag{4.22}$$

Chapter 5

Transformer design

This chapter discusses the design of the transformer used in the DAB converter. Section 5.1 explains the concept of double sided conduction, which this transformer aims to achieve. Section 5.2 discusses the implementation of this strategy to improve the efficiency of the transformer. Section 5.3 delves into the selection of core materials and the construction of the custom flexible PCB used as a winding.

5.1 Double-sided conduction (DsC)

As discussed in Section 1.1, transformers operating in high-frequency (HF) regimes pose several advantages, not limited to, high efficiency, small size and low cost. However, challenges such as increased losses arise when operating at high frequencies: core losses scale rapidly at high frequencies, and copper losses can increase due to magnetic effects like the skin and proximity effects. Hence, several design solutions are being investigated to aid in resolving these challenges. One of these solutions is the double-sided conduction (DsC) strategy.

DsC is a field-shaping technique that results in the even distribution of current on both sides of a conductor, yielding two skin-depths worth of conduction. This technique significantly reduces copper losses at high frequencies, because it A) minimizes eddy currents traveling within conductors, and B) guarantees maximum utilization of available copper area. The approach was first proposed in the context of inductors [35]. The geometry of the proposed inductor was designed to balance the H fields near each turn. By doing so, the effective conduction area was increased and DsC was achieved. The transformer proposed here leverages the same field shaping techniques to ensure double sided conduction in both windings.

[2] discusses the influence of winding arrangements on the H-field of transformers. By interleaving the windings of a transformer, depicted in Fig. 5.1a, the magneto-motive forces (MMF) can be minimized near each turn, significantly reducing the losses due to eddy current effects at HF. The interleaved winding arrangement achieves DsC by balancing the H-field on both sides of the conductors, resulting in current evenly moving towards the conductor sides.

To achieve DsC with an interleaved winding arrangement, the first and last layers, depicted in figure 5.1, must carry half the net current of every other layer. This can be done by paralleling the first and last layers of the interleaved structure or by forming each layer with half as many series-connected turns.

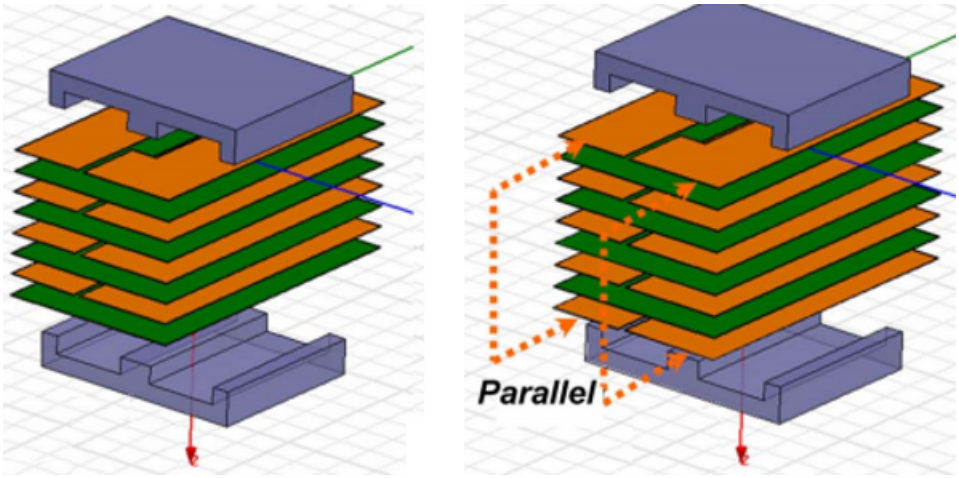


Figure 5.1: Interleaved winding structures using 3-D models of planar transformers from [2]. (a) Left, Interleaving P-S-P-S-P-S-P-S. (b) Right, DsC Interleaving 0.5P-S-P-S-P-S-P-S-0.5P. P – Primary winding, and S – Secondary winding

5.2 Applying Design Strategy to the Transformers in DAB Converter

It is easiest to achieve DsC in a transformer with high magnetizing inductance (and low magnetizing current).In a transformer with high L_m, the excitation/primary current is, ideally, the same as the secondary current factored with the transformer turns ratio, which then guarantees balanced H-fields. In addition to a high L_m, transformers designed to achieve DsC have a low leakage inductance, L_{Lk}. This occurs because of the densely interleaved transformer windings which minimize flux only coupling individual windings. Another factor that contributes to the low L_{Lk} attribute is the core design and material. This factor is further discussed in section 5.3.1.

There are three features of the transformer structure to be considered when implementing the DsC technique. The first feature is the magnetizing impedance,

Z_m of the transformer. DsC is achievable for transformers with high Z_m. Based on FEA simulations, for DsC to be achieved in a transformer, the load impedance, Z_L, has to be within 0% to 25% of Z_m. The second essential feature is the geometry of the winding structure. The turns of the windings are designed to balance the H-fields on both sides of each turn to yield 2-skin depth worth of conduction. Hence, for the design of this project's transformer windings, the thickness of the windings is twice the skin-depth of copper (Cu) at 3 MHz. The last feature is the interleaved arrangement of the windings. To achieve DsC, the first and last layer of the interleaved windings must be in parallel to carry half of the net current of every other layer. As this is a 7:1 transformer, to have an interleaved arrangement that achieves DsC, the total number of turns had to be 15. Several winding arrangements can be done for the turn counts on the transformer primary and secondary. But the most effective arrangement is having 7 turns in series on the primary (P) winding and 8 turns in parallel on the secondary (S) winding, giving an interleaved structure of S-P-S-P-S-P-S-P-S-P-S-P-S-P-S. This arrangement achieves DsC as all the secondary layers are paralleled, balancing the H-field distribution on either side of any inner layer. Section 5.3.2 explains the ease the effective winding arrangement provides in designing the turns on the type of winding material used.

Our design goals involve minimizing the size and improving efficiency of magnetic components. It is essential to select materials that will produce good performance both as individual units and when integrated together. Section 5.3 covers the material choices for the core and windings, as well as the reason for the selections.

5.3 Material Selection

Material selection is key in the design process as it determines the reliability of the design from the performance and economic standpoint. Hence, with appropriate material selection, our structure yields improved power density at its operating HF. This section dives into the materials used for the transformer components and the benefits of the chosen materials in improving the performance of the transformer.

5.3.1 Core Choice

One of the solutions to optimizing transformer operation in HF (3 - 30 MHz) regime is selecting appropriate core materials.

Selecting the best-fit core material for a desired operating HF poses its own challenges due to the limited data characterizing the performance of the material at HF. In [36], a detailed analysis is done, for a variety of commercially available HF core materials, to provide experimental data on the loss characteristics of the materials over HF range. The results in this article contributed a great deal in narrowing down suitable core materials, 3F46, PC200 and 80, with desirable characteristics at 3MHz, the switching frequency of the DAB converter.

Besides the loss characteristics of the core, two other factors that helped with determining the type of core to be used for the converter application were the core shape and the availability of the desired core. The core shape preferable for the DAB converter project was one that minimized the effect of air gaps and offered minimal winding resistance. In addition, the core had to be commercially available within the timeline for the project, narrowing down the core choices to 3F46 pot cores, PC200 RM cores and 80 EQ cores from manufacturers Ferroxcube, TDK Electronics and FairRite respectively.

In section 5.2, three essential features of the transformer were analyzed to determine conditions needed to be met for the transformer to achieve DsC; the first condition was the load impedance, Z_L had to be within (0 - 25)% of the magnetizing impedance, Z_m to ensure the transformer has a high Z_m compared to Z_L. Using the inductance factor, AL provided in the core datasheet and 5.1, Z_m was calculated for each core option to ensure that double sided conduction would be achieved. The primary referred magnetizing inductance is:

$$Z_m = (2\pi f_s w)_L \, N_p^2) \tag{5.1}$$

where f_{sw} is the switching frequency, N_p is the number of primary turns, and A_L is the one turn inductance.

One of the project requirements was to have a maximum transformer loss of 2% at full load power (100W). Two transformers are used in the converter, meaning each must have a maximum of 1W loss. The loss in each transformer comes both copper and core loss. Hence, the target loss was set as a maximum of 0.5W for

each of the loss components. To estimate the theoretical core loss, P_{Cr} of the transformer, the loss vs flux density characteristic curves of the core, provided by the core manufacturer was used. The flux density, B was calculated using 5.2, where A_C is the effective cross-sectional area of the core.

$$B = \frac{V_p}{(4 * f_s w * N_p * A_c)} \tag{5.2}$$

From the characteristic curve, the log-log equation (5.3) was derived to relate P_{Cr} to B and to estimate P_{Cr}. m is the approximate slope of the log-log plot.

$$P_{cr} = \left(\frac{P_{cr0}}{B_0^m}\right) \times B^m \tag{5.3}$$

Another method used to estimate P_{cr} was using the generalized Steinmetz's equation (GSE), eq.5.4. The Steinmetz parameters were extrapolated using ANSYS Maxell 2D [4].

$$P_{cr} = C_m * f_{sw}^{\alpha} * Bac^{\beta} \left(\frac{mW}{cm^3}\right) \tag{5.4}$$

where C_m, α, and β are the Steinmetz parameters, f_{sw} is the switching frequency in Hertz (Hz), and B_{ac} is maximum amplitude of the flux density in Tesla (T).

From the core loss results, among other results, the chosen core for the transformer structure is a PC200 RM core from TDK Electronics with dimensions (20.3 x 8 x 13.5) mm.

5.3.2 Winding Design

The DsC technique yields 2-skin depth worth of conduction per turn at HFs, hence, in designing the windings, a minimum thickness of 2-skin depth of copper is desirable to meet this yield. We considered the use of copper foils which come in a variety of thickness, less or greater than 2-skin depth of copper. However, this winding material poses its own challenges with cutting precision and finding the best fit (size) dielectric material between the primary and secondary winding. In the case a laser cutter is used for precise cuts, two main areas of concern will be the reflection of the laser back on itself, which will depend on the way the material is cut, and as precision is key, several test runs will have to be performed to determine

the extra mm that will account for any potential loss of material during the cut. Ultimately, the laser cutter route depends on the availability of the machine and its ability to cut relatively low dimensions. As a result, a novel idea is explored for the transformer design: utilizing a flexible printed circuit board (flex PCB) as the winding material to replace conventional options.

The flex PCB has great potential as an alternative to copper foil for winding. The winding structure is easily designed using PCB design software, and precisely cut out, with no opportunity for human error. Most manufacturers are able to print flexible copper thicknesses up to 3oz (254 um) with at most 6 conductive layers. In our case, a 2-layer board is required to represent the primary and secondary windings of the transformer. The closest available copper thickness to 2-skin depth of copper at 3MHz was 2oz of copper. Per calculations and simulations, it was verified that the slight decrease in copper thickness would result in a increase in loss by slightly less than 10%. Furthermore, the flex PCB comes with in-built dielectric materials between the copper layers which eliminates the need to find the right dielectric material thickness and inserting the material between the materials.

Transformer simulations for DsC were done for instances with evenly spaced windings, that is, the dielectric material has the same thickness between each winding. However, this is not the case for 2-layer flex PCBs as seen in 5.2. When the flex PCB is wound about the core's center post, the spacing between the windings has a sequence of (50-25-100-25-100...) microns Per simulation, with the uneven spacing sequence, the transformer still achieved DsC. Furthermore, the percent difference, for the copper loss between the even and uneven spacing, was calculated. For even spacings of 25 microns and 50 microns the copper loss, compared to that for the uneven spacing, had less than a 5% decrease. While the even spacing of 100 microns had about a 5.5% increase in copper loss when compared to that from the uneven spacing. This percent difference in copper losses proved the uneven spacing will not be a detriment to the transformer achieving DsC.

The primary winding is placed on the top copper layer of the flex PCB. It consists of 7 turns in series, hence, one sheet of copper with a total length equivalent to the sum of the length of each turn. The secondary winding is designed on the bottom copper layer of the flex PCB. It consists of 8 turns in parallel, hence, 8 separate sheets of copper, each the length of the corresponding turn. To meet the requirement set by the PCB manufacturer, the spacing between each sheet

top coverlay	PI	25um
	Adhesive	25um
top copper layer	Copper	70um(Finished Copper thickness 70um)
	Adhesive	0um
	PI	25um
	Adhesive	0um
bottom copper layer	Copper	70um(Finished Copper thickness 70um)
bottom coverlay	Adhesive	25um
	PI	25um
Total thickness		**265um**

Figure 5.2: 2-layer stack-up for flex PCB used for the design of the transformer windings. The dielectric material, between the copper layers, gives an uneven spacing sequence of (50-25-100-25-100...)µm.

is 0.16mm. To connect the flex PCB to the transformer connectors on the DAB converter, two connecting tabs, per copper sheet, were created.

A factor to check the flexibility of the PCB is the bend radius. The bend radius must be known to ensure the stress point – the point where the copper layer fractures if the flex PCB is greatly extended – of the flex PCB is never reached. The smaller the bend radius, the greater the material's flexibility. The bend radius of flex PCBs is ideally between 10-12 times the flex material thickness. In our design, the bend radius is between (2.65 - 3.18) mm, which is less than the smallest radius (4.00mm) of one of the turns. 5.3 shows images of the flex PCB design.

The DsC interleaved winding structure has the form S-P-S-P-S-P-S-P-S-P-S-P-S-P-S. Each S-P and P-S pair resembles a capacitor and will have a winding capacitance. However, this parasitic capacitance, on the order of 4.00 pF, is negligible.

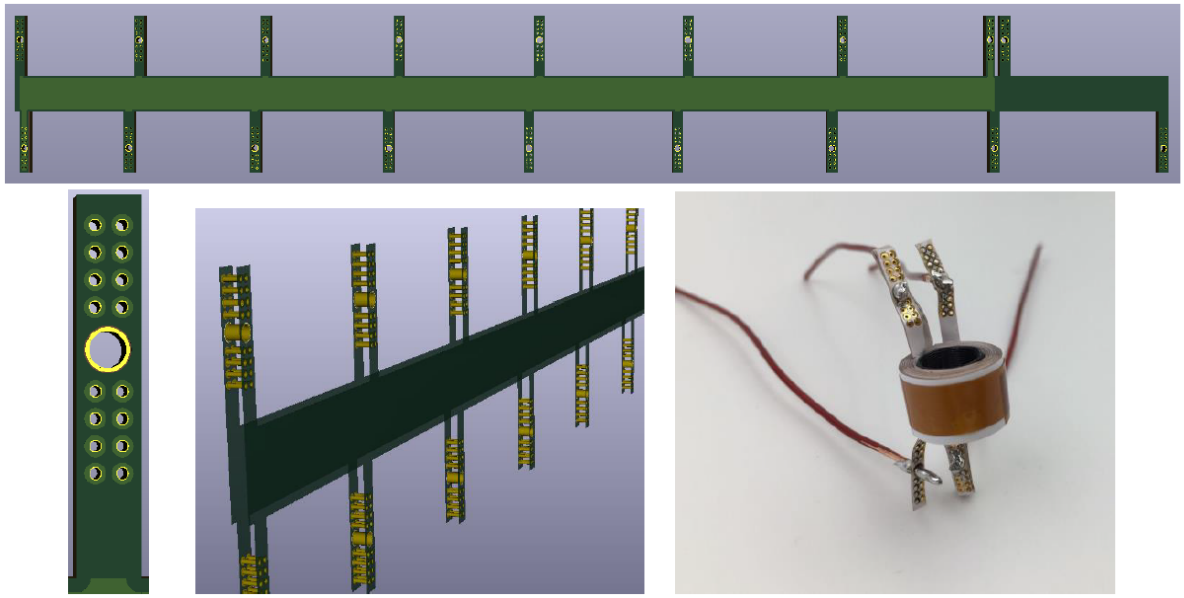


Figure 5.3: Top, KiCAD layout of flex PCB with dimensions of 269.75 x 36.4 mm (including height of soldering tabs). Bottom right, soldering tabs with dimensions 2.35 x 14mm, and vias diameters 1.35 mm (center) and 0.4mm (small). Bottom center, side view of flex PCB with vias. Bottom right, wounded flex PCB on core bobbin.

Chapter 6

Controller Scheme

In an n-module ISOP system, the input voltage and output current are reduced by a factor of n for each module. This reduces current and voltage stress of the switching device and allows us to expand to high-frequency, high-voltage capability using low voltage FETs. However, in an ISOP system, the difference between module parameters can lead to voltage unbalance and current issues [37]. To avoid over-stressing of the circuit components, it is necessary to ensure input voltage and output current sharing among the modules. The output voltage also needs to be regulated in the converter. Thus, for an ISOP system a control scheme is designed to regulate the systems output voltage and enforce input voltage and output current sharing. ISOP control scheme are classified as natural power balance scheme[38][39] and specific sharing scheme[40][41][42][43][44]. Natural power balance scheme have been observed to show poor input voltage and output current sharing characteristics[45]. Few of the sharing schemes focus on output side i.e. enforcing output current sharing among the modules. In [46]of output current sharing loop is examined and it is concluded that output current sharing scheme doesn't lead to a stable operation. Hence, in this study the novel input voltage sharing (IVS) strategy proposed in [46]. This control strategy consists of (n-1) individual input voltage sharing regulator (IVSR) loops and a output voltage regulator (OVR) loop. The loops interact among themselves so to make the design process simpler the network is decoupled to non-interacting loops. Control-to-input and control-to-output transfer functions are required to design control-loop compensation for IVSR and OVR. Small-signal modeling technique is used to approximate the converter circuit with non-linear devices with linear equations and derive the transfer functions. The generalized average model method discussed in [47][48][49] is explored below.

6.1 Small Signal Model

6.1.1 Small signal modelling of DAB converter

The circuit diagram of a dc-dc DAB converter is given in Fig 2.1. It consists of two H-bridges and a high-frequency transformer. The high-frequency transformer provides both galvanic isolation and energy storage through winding leakage inductance. Due to the total of eight switching elements in this topology, the number of different control methods is very high and there are several degrees of freedom that can be used for optimization. The given dc-dc DAB converter is controlled using the single phase-shift modulation (SPSM) technique operating at a fixed switching frequency and fixed 50% duty ratio. The power is being transferred from the leading bridge i.e. the primary bridge to the lagging bridge i.e. the secondary bridge. The power delivered is expressed in eqn 6.1

$$P = \frac{nV_{in}V_o}{2f_sL_k}d(1-d) \tag{6.1}$$

where n is the turns ratio of the high-frequency transformer, V_{in} and V_o are the converter input and output voltages, respectively, $d = \phi/\pi$ the phase shift ratio between two bridges, and $d \in [-1, 1]$, f_s switching frequency, L_k leakage inductor of the high-frequency transformer, referred to the input side.

The generalized model for DAB converters is derived based on the following assumptions:
[1] The transformer magnetizing current is not significant.
[2] The voltage drop across transistordiode pairs is negligible.
[3] The transistor switching transients are negligible. The given DAB is controlled using PSM techniques, the voltage at the transformer input side, v_p, can be expressed as:

$$v_p(\tau) = s_1(\tau)v_{in}(\tau) \tag{6.2}$$

where $s_1(\tau)$, the switching function at primary bridge, is given below eqn 6.3

$$s_1(\tau) = \begin{cases} 1, & 0 \leq \tau \leq \frac{T}{2} \\ -1, & \frac{T}{2} \leq \tau \leq T \end{cases} \tag{6.3}$$

where T= $1/f_s$ is the switching period of transistors. Similarly, the voltage at the transformer output side, v_s, can be expressed as

$$v_s(\tau) = s_2(\tau)v_0(\tau) \tag{6.4}$$

where $s_2(\tau)$, the switching function at secondary bridge, is given below:

$$s_2(\tau) = \begin{cases} 1, & \frac{dT}{2} \leq \tau \leq \frac{T}{2}(1+d) \\ -1, & 0 \leq \tau \leq \frac{dT}{2} \; or \; \frac{T}{2}(1+d) \leq \tau \leq T \end{cases} \tag{6.5}$$

To achieve the final goal of input voltage sharing and output voltage control in the modular system, the converter input and output voltage, $v_{in}(\tau)$ and $v_o(\tau)$ respectively, and the transformer current $i_t(\tau)$ are selected as the state variables. The state space equations for the given DAB converter are shown in equations 6.6 - 6.8.

$$\frac{dv_{in}(\tau)}{d\tau} = \frac{i_{in}(\tau)}{C_{in}} - \frac{s_1(\tau)i_t(\tau)}{C_{in}} \tag{6.6}$$

$$\frac{di_t(\tau)}{d\tau} = -\frac{R_t i_t(\tau)}{L_t} + \frac{s_1(\tau)v_{in}(\tau)}{L_t} - \frac{ns_2(\tau)v_o(\tau)}{L_t} \tag{6.7}$$

$$\frac{dv_o(\tau)}{d\tau} = -\frac{v_o(\tau)}{RC_o} + \frac{ns_2(\tau)i_t(\tau)}{C_0} \tag{6.8}$$

These time-varying and non-linear equations are averaged to derive the small-signal equivalent circuit of a given topology with linear time-invariant equations. In the averaging method a state variable $x(\tau)$ is represented using its Fourier series, during

the time interval $t - T \leq \tau \leq t$

$$x(\tau) = \sum_{j=-\infty}^{\infty} \langle x(\tau) \rangle_k e^{jkw_s\tau} \tag{6.9}$$

where $w_s = 2\pi f_s$, and complex number $\langle x(\tau) \rangle_k$ is the k^{th} coefficient in the Fourier series.

$$\langle x(\tau) \rangle_k = \frac{1}{T} \int_{t-T}^{t} x(\tau) e^{-jkw_s t} \tag{6.10}$$

$$\langle x(\tau) \rangle_k = \frac{1}{T} \int_{t-T}^{t} x(\tau) w_s \cos(kw_s t) d\tau - \frac{j}{T} \int_{t-T}^{t} x(\tau) w_s \sin(kw_s t) d\tau \tag{6.11}$$

The conventional state space averaging only consider dc terms (k = 0) assuming low ripple in state variables. On the other hand, in DAB converter the transformer current i_t is purely ac, i.e. high ripple and dc term is zero so instead of conventional averaging the generalized state space averaging is used here as it does not assume that the ripples of state variables are small and hence, keeps more terms in the Fourier series of state variables. This technique discards less information and might be more accurate. In this study, the zeroth and first component (k = 0,1,-1) are considered.

From ref [48] and [50] the derivative of k^{th} coefficient of x is

$$\frac{d}{dt} \langle x(t) \rangle_k \simeq \langle \frac{dx}{dt} \rangle_k (t) - jkw_s \langle x \rangle_k (t) \tag{6.12}$$

where $\langle \frac{dx}{dt} \rangle_k$ represents the average of the differential of a state variable. The k^{th} coefficient of the product of two variables x and y is

$$\langle xy \rangle_k \simeq \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i} \langle y \rangle_i \tag{6.13}$$

The 1 and -1 coefficient of the fourier series are considered as complex conjugates. The zeroth and first coefficient of the product of two variables x and y are

$$\langle xy \rangle_0 \simeq \langle x \rangle_0 \langle y \rangle_0 + 2(\langle x \rangle_{1R} \langle y \rangle_{1R} + \langle x \rangle_{1I} \langle y \rangle_{1I}) \tag{6.14}$$

$$\langle xy\rangle_{1R} \simeq \langle x\rangle_0\langle y\rangle_{1R} + \langle x\rangle_{1R}\langle y\rangle_0 \tag{6.15}$$

$$\langle xy\rangle_{1I} \simeq \langle x\rangle_0\langle y\rangle_{1I} + \langle x\rangle_{1I}\langle y\rangle_0 \tag{6.16}$$

Applying these operations to our original state space equations shown in eqns. 6.6 - 6.8, we get the equations for zeroth and first coefficient of state variables:

$$\frac{d}{dt}\langle v_{in}\rangle_0 = \frac{\langle i_{in}\rangle_0}{C_{in}} - \frac{\langle s_1\rangle_0\langle i_t\rangle_0}{C_{in}} - \frac{2\langle s_1\rangle_{1R}\langle i_t\rangle_{1R}}{C_{in}} - \frac{2\langle s_1\rangle_{1I}\langle i_t\rangle_{1I}}{C_{in}} \tag{6.17}$$

$$\frac{d}{dt}\langle v_{in}\rangle_{1R} = \frac{\langle i_{in}\rangle_{1R}}{C_{in}} - \frac{\langle s_1\rangle_0\langle i_t\rangle_{1R}}{C_{in}} - \frac{\langle s_1\rangle_{1R}\langle i_t\rangle_0}{C_{in}} + w_s\langle v_{in}\rangle_{1I} \tag{6.18}$$

$$\frac{d}{dt}\langle v_{in}\rangle_{1I} = \frac{\langle i_{in}\rangle_{1I}}{C_{in}} - \frac{\langle s_1\rangle_0\langle i_t\rangle_{1I}}{C_{in}} - \frac{\langle s_1\rangle_{1I}\langle i_t\rangle_0}{C_{in}} - w_s\langle v_{in}\rangle_{1R} \tag{6.19}$$

$$\begin{aligned}\frac{d}{dt}\langle i_t\rangle_0 = &- \frac{R_t\langle i_t\rangle_0}{L_t} + \frac{\langle s_1\rangle_0\langle v_{in}\rangle_0}{L_t} + \frac{2}{L_t}\big(\langle s_1\rangle_{1R}\langle v_{in}\rangle_{1R} + \langle s_1\rangle_{1I}\langle v_{in}\rangle_{1I}\big)\\ &- \frac{n\langle s_2\rangle_0\langle v_o\rangle_0}{L_t} - \frac{2n}{L_t}\big(\langle s_2\rangle_{1R}\langle v_o\rangle_{1R} + \langle s_2\rangle_{1I}\langle v_0\rangle_{1I}\big)\end{aligned} \tag{6.20}$$

$$\begin{aligned}\frac{d}{dt}\langle i_t\rangle_{1R} = &- \frac{R_t\langle i_t\rangle_{1R}}{L_t} + w_s\langle i_t\rangle_{1I}\\ &+ \frac{1}{L_t}\big(\langle s_1\rangle_0\langle v_{in}\rangle_{1R} + \langle s_1\rangle_{1R}\langle v_{in}\rangle_0\big)\\ &- \frac{n}{L_t}\big(\langle s_2\rangle_0\langle v_o\rangle_{1R} + \langle s_2\rangle_{1R}\langle v_o\rangle_0\big)\end{aligned} \tag{6.21}$$

$$\begin{aligned}\frac{d}{dt}\langle i_t\rangle_{1I} = &- \frac{R_t\langle i_t\rangle_{1I}}{L_t} - w_s\langle i_t\rangle_{1R}\\ &+ \frac{1}{L_t}\big(\langle s_1\rangle_0\langle v_{in}\rangle_{1I} + \langle s_1\rangle_{1I}\langle v_{in}\rangle_0\big)\\ &- \frac{n}{L_t}\big(\langle s_2\rangle_0\langle v_o\rangle_{1I} + \langle s_2\rangle_{1I}\langle v_o\rangle_0\big)\end{aligned} \tag{6.22}$$

$$\frac{d}{dt}\langle v_o\rangle_0 = -\frac{\langle v_o\rangle_0}{RC_o} + \frac{n\langle s_2\rangle_0\langle i_t\rangle_0}{C_o} + \frac{2n\langle s_2\rangle_{1R}\langle i_t\rangle_{1R}}{C_o} + \frac{2n\langle s_2\rangle_{1I}\langle i_t\rangle_{1I}}{C_o} \tag{6.23}$$

$$\frac{d}{dt}\langle v_o\rangle_{1R} = -\frac{\langle v_o\rangle_{1R}}{RC_o} + \frac{n\langle s_2\rangle_0\langle i_t\rangle_{1R}}{C_o} + \frac{n\langle s_2\rangle_{1R}\langle i_t\rangle_0}{C_o} + w_s\langle v_o\rangle_{1I} \tag{6.24}$$

$$\frac{d}{dt}\langle v_o\rangle_{1I} = -\frac{\langle v_o\rangle_{1I}}{RC_o} + \frac{n\langle s_2\rangle_0\langle i_t\rangle_{1I}}{C_o} + \frac{n\langle s_2\rangle_{1I}\langle i_t\rangle_0}{C_o} - w_s\langle v_o\rangle_{1R} \tag{6.25}$$

Where, assuming that the dynamics of input voltage and load are slow compared to the DAB converter $\langle v_{in}\rangle_0 = V_{in}$ $\langle v_{in}\rangle_{1R} = \langle v_{in}\rangle_{1I} = 0, \langle i_{in}\rangle_0 = I_{in}$ $\langle i_{in}\rangle_{1R} = \langle i_{in}\rangle_{1I} = 0$, *and* $\langle i_t\rangle_0 = 0$. The given topology is controlled using SPSM techniques therefore, the switching functions $s_1(t)$ *and* $s_2(t)$ have fixed 50% duty ratio. $\langle s_1\rangle_0 = \langle s_2\rangle_0 = 0$

$$\langle s_1\rangle_{1R} = 0 \quad \langle s_1\rangle_{1I} = -\frac{2}{\pi} \tag{6.26}$$

$$\langle s_2\rangle_{1R} = -\frac{2\sin d\pi}{\pi} \quad \langle s_2\rangle_{1I} = -\frac{2\cos d\pi}{\pi} \tag{6.27}$$

After substitution, the final equations of the zeroth and first coefficient of state variables are expressed in the matrix form in equation 6.28,
where $G = [v_{in0}\ v_{o0}\ i_{t1R}\ i_{t1I}\ v_{in1R}\ v_{in1I}\ v_{o1R}\ v_{o1I}\ i_{t0}]^T$

$$\frac{dG}{dt} = \begin{bmatrix} 0 & 0 & 0 & \frac{4}{\pi C_{in}} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{RC_o} & -\frac{4n\sin d\pi}{\pi C_o} & -\frac{4n\cos d\pi}{\pi C_o} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{2n\sin d\pi}{\pi L_t} & -\frac{R_t}{L_t} & w_s & 0 & 0 & 0 & 0 & 0 \\ -\frac{2}{\pi L_t} & \frac{2n\cos d\pi}{\pi L_t} & w_s & -\frac{R_t}{L_t} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & w_s & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -w_s & 0 & 0 & 0 & -\frac{2}{\pi C_{in}} \\ 0 & 0 & 0 & 0 & 0 & w_s & -\frac{1}{RC_o} & 0 & \frac{2n\sin d\pi}{\pi C_o} \\ 0 & 0 & 0 & 0 & -w_s & 0 & 0 & -\frac{1}{RC_o} & \frac{2n\cos d\pi}{\pi C_o} \\ 0 & 0 & 0 & 0 & 0 & -\frac{4}{\pi L_t} & \frac{4n\sin d\pi}{\pi L_t} & \frac{4n\cos d\pi}{\pi L_t} & -\frac{R_t}{L_t} \end{bmatrix} G + \begin{bmatrix} \frac{1}{C_{in}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} I_{in} \tag{6.28}$$

It can be observed that the dynamic of $v_{in0}\ v_{o0}\ i_{t1R}\ i_{t1I}$ is independent of the rest of the system so eqn. 6.28 can be converter to eqn. 6.29, a four-order model where $X = [v_{in0}\ v_{o0}\ i_{t1R}\ i_{t1I}]^T$

$$\frac{dX}{dt} = \begin{bmatrix} 0 & 0 & 0 & \frac{4}{\pi C_{in}} \\ 0 & -\frac{1}{RC_o} & -\frac{4n\sin d\pi}{\pi C_o} & -\frac{4n\cos d\pi}{\pi C_o} \\ 0 & \frac{2n\sin d\pi}{\pi L_t} & -\frac{R_t}{L_t} & w_s \\ -\frac{2}{\pi L_t} & \frac{2n\cos d\pi}{\pi L_t} & w_s & -\frac{R_t}{L_t} \end{bmatrix} X + \begin{bmatrix} \frac{1}{C_{in}} \\ 0 \\ 0 \\ 0 \end{bmatrix} I_{in} \tag{6.29}$$

The small-signal averaged model is a good tool for controller design and stability analysis as the s-domain small-signal models can be used to study the frequency response of the converter. To obtain the small signal model the averaged state equations in are perturbed to yield steady-state and dynamic terms. The product of any ac terms are eliminated and thr equations are trasformed into s-domain to solve for converter transfer functions. Assuming input voltage constant, a small pertubation in d leads to the following deviation in state variables $v_{o0}\ i_{t1R}\ i_{t1I}$

$$\begin{aligned} \hat{d} &= d - D \\ \hat{v}_{o0} &= v_{o0} - V_{o0} \\ \hat{i}_{t1R} &= i_{t1R} - I_{t1R} \\ \hat{i}_{t1I} &= i_{t1I} - I_{t1I} \end{aligned} \tag{6.30}$$

where Z is the steady state, z is the large signal state and $\hat{z}$ is the small signal

state of variable x. The steady state values of v_{in0} v_{o0} i_{t1R} i_{t1I} can be obtained by equating equation to zero.

$$\frac{dX}{dt} = 0 \tag{6.31}$$

Therefore,

$$\frac{d\hat{X}}{dt} = A\hat{X} + B\hat{d} \tag{6.32}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{4}{\pi C_{in}} \\ 0 & -\frac{1}{RC_o} & -\frac{2y}{C_o} & -\frac{2y}{C_o} \\ 0 & \frac{y}{L_t} & -\frac{R_t}{L_t} & w_s \\ -\frac{2}{\pi L_t} & \frac{x}{L_t} & -w_s & -\frac{R_t}{L_t} \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ z \\ g \\ h \end{bmatrix} \tag{6.33}$$

where,

$$\begin{aligned} x &= \frac{2n\cos D\pi}{\pi} \quad y = \frac{2n\sin D\pi}{\pi} \\ z &= \frac{4n}{C_o}\big(I_{t1I}\sin D\pi - I_{t1R}\cos D\pi\big) \\ g &= \frac{2n\cos D\pi}{L_t}V_o \quad y = \frac{2n\sin D\pi}{L_t}V_o \end{aligned} \tag{6.34}$$

Transforming eq 6.34 to s-domain, the $\hat{d}$ to $\hat{X}$ can be expressed as:

$$\frac{\hat{X}}{\hat{d}} = (sI - A)^{-1}B \tag{6.35}$$

Solving eq 6.35 leads us to the converters control-to-input $G_{vid}(s)$ and control-to-output transfer function $G_{vod}(s)$. The converters output impedance $Z_{out}(s)$ is obtained by adding a current source at the load, to incorporate for $\hat{i_o}$ variations, and rewrite the state space equations.

6.1.2 Modelling of DAB based ISOP converter

An ISOP modular system demands a multi-objective control strategy to ensure equal sharing of input voltage and output current among the constituent con-

verters. Assuming all the DAB converters have same circuit parameters, the single DAB converter modeling is continued to derive control to output voltage and control to module input voltage transfer functions. In the given two DAB ISOP system, the first DAB module is set as reference and the difference between state variables in second DAB module and reference is expressed as

$$\frac{d}{dt}(\hat{X}_2 - \hat{X}_1) = A(\hat{X}_2 - \hat{X}_1) + B(\hat{d}_2 - \hat{d}_1) \tag{6.36}$$

Transforming eqn 6.36 to s-domain, we have

$$\hat{X}_2 - \hat{X}_1 = (sI - A)^{-1}B(\hat{d}_2 - \hat{d}_1)$$

So, the difference between input voltage of DAB modules is

$$\begin{aligned} \hat{V}_{in0,2} - \hat{V}_{in0,1} &= G_{vid}(s)(\hat{d}_2 - \hat{d}_1) \\ \hat{V}_{in0,2} &= G_{vid}(s)(\hat{d}_2 - \hat{d}_1) + \hat{V}_{in0,1} \end{aligned} \tag{6.37}$$

When $\sum \hat{V}_{in0} = 0$, then $\hat{V}_{in0,1} = -\hat{V}_{in0,2}$, substituting this into eqn 6.37, we have

$$\begin{aligned} \hat{V}_{in0,1} &= \frac{G_{vid}(s)}{2}(\hat{d}_1 - \hat{d}_2) \\ \hat{V}_{in0,2} &= \frac{G_{vid}(s)}{2}(\hat{d}_2 - \hat{d}_1) \end{aligned} \tag{6.38}$$

Expressing eqn 6.38 in matrix form

$$\begin{bmatrix} \hat{V}_{in0,1} \\ \hat{V}_{in0,2} \end{bmatrix} = G_{vid}(s) \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix}$$

As it is a ISOP system, the output voltage across each DAB module is same. The control-to-output transfer function for the ISOP converter is sum of that in every DAB module

$$\hat{V}_{o0} = G_{vod}(s)(\hat{d}_1 + \hat{d}_2) \tag{6.39}$$

From eqn 6.38 and 6.39, we can obtain

$$\begin{bmatrix} \hat{V}_{in0,1} \\ \hat{V}_{o0} \end{bmatrix} = H \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \tag{6.40}$$

where,

$$H = \begin{bmatrix} \frac{G_{vid}(s)}{2} & -\frac{G_{vid}(s)}{2} \\ G_{vod}(s) & G_{vod}(s) \end{bmatrix}$$

The system diagram representing eqn 6.40 is shown in Fig. 6.1, where $G_{vc}(s), G_{vo}(s)$ are the IVSR and OVR loop compensation transfer function, and $Z_{out}(s)$ is converters output impedance

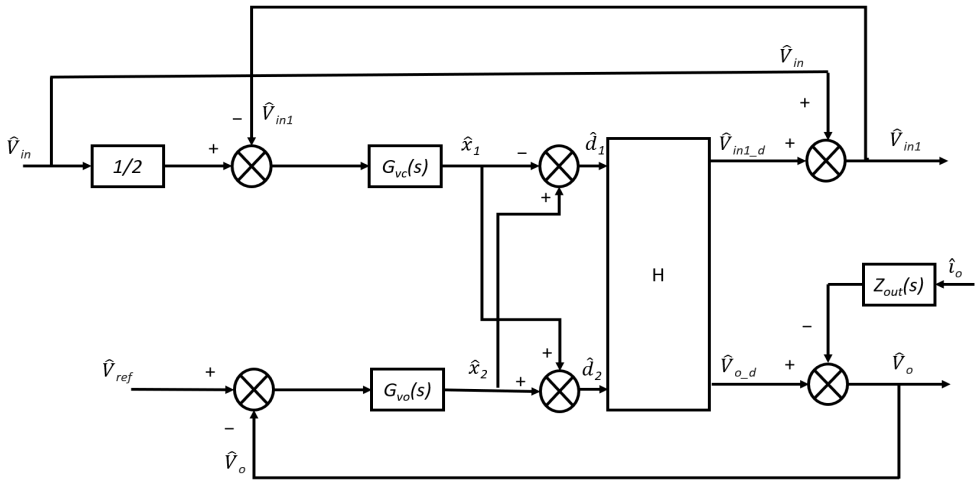


Figure 6.1: System block diagram of ISOP converter with IVS control strategy

From Fig. 6.1 a relation between $\hat{d}_1, \hat{d}_2$ and $\hat{x_1}, \hat{x_2}$ is found as follows

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} \tag{6.41}$$

Incoorporating eqn 6.41 into eqn 6.40, we can get a simpler version of the

block system in Fig 6.1

$$\begin{bmatrix} \hat{V}_{in0,1} \\ \hat{V}_{o0} \end{bmatrix} = \begin{bmatrix} -G_{vid}(s) & 0 \\ 0 & 2G_{vod}(s) \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \tag{6.42}$$

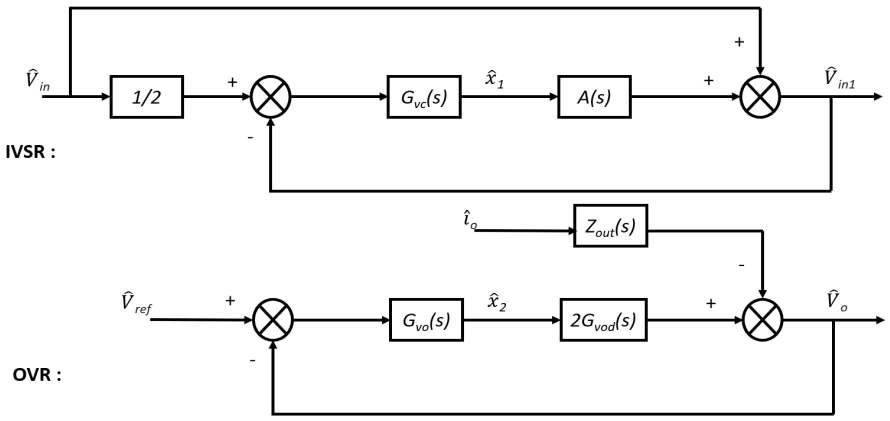


Figure 6.2: Decoupled loops diagram of ISOP converter with IVS control strategy

Fig 6.2 represents eqn 6.42 and shows that the input voltage sharing loop and output voltage regulating loop are decoupled and can be designed independently.

From eqn 6.35 and table 6.1, the control-to-input, control-to-output transfer functions, and the converters output impedance are as follows:

$$G_{vid}(s) = \frac{5.022e-11s + 1.23e-05}{2.45e-16s^2 + 4.68e-11s + 4.655e-08}$$
$$G_{vod}(s) = \frac{2.66e-12s + 7.98e-09}{3e-18s^2 + 5.73e-13s + 5.7e-10}$$
$$Z_{out}(s) = \frac{-1.25e04s^3 - 0.002761s^2 - 4.443e18s - 1.202e09}{s^4 + 1.929e05s^3 + 3.598e14s^2 + 6.856e19s + 6.033e22}$$

Parameter	single DAB converter	2-DAB module ISOP system
V_{in}	24V	48V
V_o	1.8V	1.8V
C_{in}	80 µF	80 µF
C_o	80 µF	160 µF
L_t	103 nH	103 nH
R_t	0 Ω	0 Ω
R_L	0.0648 Ω	0.0324 Ω
f_s	3MHz	3MHz
n:1	6.6667: 1	6.6667:1
P	50W	100W

Table 6.1: Circuit parameters

6.2 Controller design

6.2.1 DAB converter

In a single DAB converter only the output voltage needs to be regulated. The derived control-to-output transfer function $G_{vod}(s)$ is shown in Fig.6.3. It is observed that the $G_{vod}(s)$ is stable with 138 kHz crossover frequency and phase margin of 102°. This system is an open-loop system, i.e., a non-feedback controller; it does not use a feedback loop to determine if its output has achieved the desired goal. An open-loop system cannot correct any errors that it makes or correct for outside disturbances. Whereas, a closed-loop system has a feedback loop which ensures the controller exerts a control action to give a process output the same as the set point. This kind of feedback control system can be established by combining a compensator's feedback loop with the feed-forward (open-loop) system. The compensator primarily has to compensate whatever difference or error remains between the setpoint and the system response to the open-loop control. Working together, the combined open-loop feed-forward system and closed-loop compensator can help us achieve a more responsive control system.

A PID compensator shown in Fig. 6.4 comprises three distinct blocks, each processing the error signal with the respective functions: proportional, integral, and derivative. The behavioral parameters of a control system such as rise time, damping ratio, or response time can be tuned by individually adjusting the block gains.

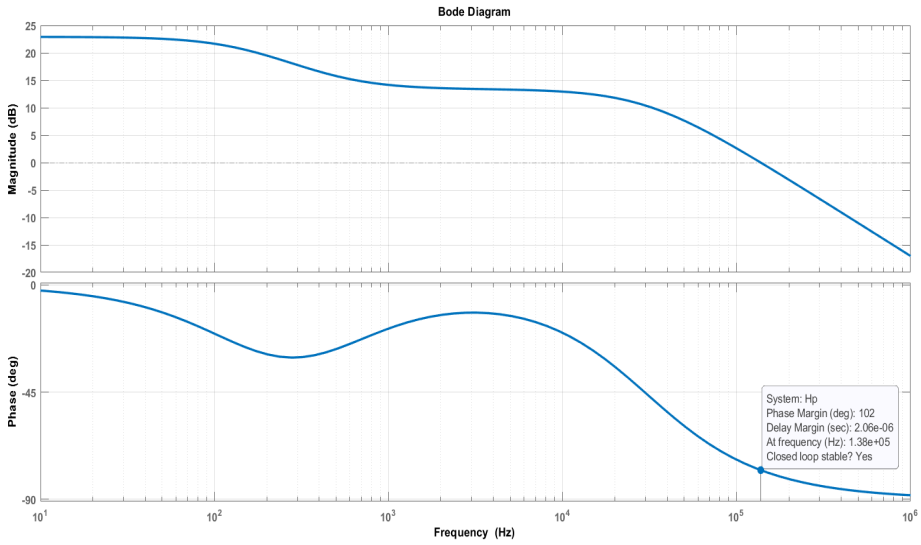


Figure 6.3: Bode plot of Control-to-output transfer function

The three blocks of PID produce outputs with the following nature:

- P : proportional to the error at the instant t, "present" error.
- I : proportional to the integral of the error up to the instant t,"past" error.
- D : proportional to the derivative of the error at the instant t,"future" error.

The transfer function $G_c(s)$ of the PID controller is :

$$G_c(s) = K_p + \frac{K_i}{s} + K_d s \tag{6.43}$$

Implementing the derivative term as recommended in equation 6.43 results in extreme sensitivity to incoming noises or perturbations. To prevent high-frequency noise from coming in, a pole at N rad/s is included that safely excludes the upper portion of the frequency spectrum. Additional pole in the PID equation, as in equation 6.44 gives birth to the filtered-PID.

$$G_c(s) = K_p + \frac{K_i}{s} + \frac{N K_d s}{(N + K_d s)} \tag{6.44}$$

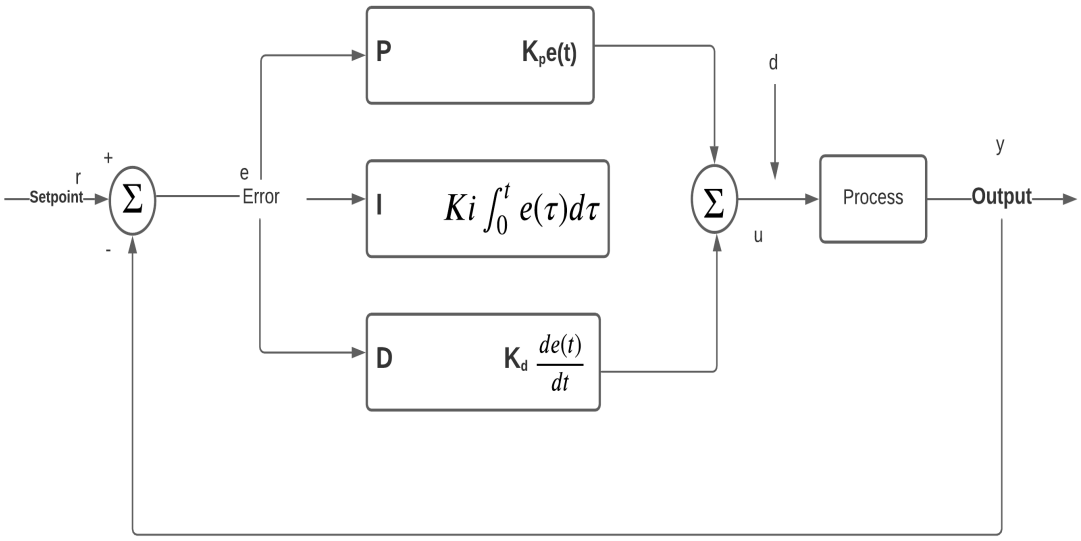


Figure 6.4: PID implementation showing three distinct blocks

A filtered PID is same as a compensator setting a double zero, an origin pole, and a high-frequency pole. Equation 6.44 is converted to pole-zero form :

$$G_c(s) = \frac{(1 + s/w_{z1})(1 + s/w_{z2})}{\frac{s}{w_{p0}}(1 + \frac{s}{w_{p1}})} \tag{6.45}$$

Equation 6.45 help us bridge a relation between the PID coefficients and the compensators pole and zeros. A PI compensator is basically the PID equation excluding the derivative term and transforms into a simpler expression. Similarly the PI compensator equation can be expressed as a compensator setting a single zero, an origin pole.

$$G_c(s) = K_p + \frac{K_i}{s} = \frac{1 + s/w_{z1}}{\frac{s}{w_{p0}}} \tag{6.46}$$

PID/PI compensator design can be done using standard PID design techniques Ziegler and Nichols experimental processes,etc or the compensator is designed with direct poles-zeros placement and then converted to PID form. The poles and zeros are positioned according to the desired crossover frequency and phase margin [51].

The latter method is used in this study. Following steps are followed to derive the compensator transfer function:

- Identify the magnitude and argument of the transfer function Hp(s) at the desired crossover frequency.
- Place a origin pole in the compensator to offer high DC gain
- Identify the position of pole-zero pair and the gain to force the crossover at desired frequency f_c and ensure desired open-loop phase margin.

Based on boost required to ensure the target margin at f_c there are three types of compensator:

$$boost = PM - argH(f_c) - 90^\circ \tag{6.47}$$

- Type 1: 1 origin pole, no phase boost required
- Type 2: 1 origin pole and 1 pole-1 zero, phase boost required up to 90°
- Type 3: 1 origin pole and 2 pole- 2 zero, phase boost required up to 180°

The switching frequency for the DAB converter discussed above is 3 MHz. The desired crossover frequency f_c is set as one-twelfth of the switching frequency and the target open-loop phase margin is 60°. From Fig. 6.3 the magnitude and argument of the transfer function $G_{vod}(s)$ at f_c are identified as:

$$f_c = 250\,\text{kHz}; Gvod_{f_c} = -5.03dB; P_{f_c} = -83.17^\circ; \tag{6.48}$$

As the phase boost required is less than 90°, type 2 compensator is designed. A pole-zero pair can create a phase boost upto 90°. To ensure maximum boost at the crossover f_c, the pole-zero $(f_p - f_z)$ is positioned accordingly. A origin pole f_{p0} is added to ensure the compensator nullifies the transfer function $G_{vod}(s)$ magnitude $Gvod_{f_c}$ at f_c,and thus sets the cross-over frequency of loop-transfer function $T_{ol}(s) = H_p(s)G_c(s)$ at f_c.

$$boost = (\frac{f_c}{f_z}) - (\frac{f_c}{f_p}) \tag{6.49}$$

$$f_c = \sqrt{f_z f_p} \tag{6.50}$$

$$f_{p0} = f_z 10^{\left(\frac{-G_{f_c}}{20}\right)} \tag{6.51}$$

$$G_c(s) = \frac{(1 + s/w_z)}{s/w_{p0}(1 + s/w_p)} \tag{6.52}$$

$$G_c(s) = \frac{a_1 s + a_0}{b_2 s^2 + b_1 s} \tag{6.53}$$

where, $a_1 = 1.912e-06$ $a_0 = 1$ $b_2 = 2.271e-13$ $b_1 = 1.072e-06$

$G_c(s)$ is the type 2 compensator transfer function. Fig. 6.5 shows the bode plots of compensated and uncompensated control-to-output transfer function for the given DAB converter i.e. $G_{vod}(s)$ and the loop transfer function $T_{ol}(s)$. The target of crossover frequency of loop transfer function equal to 250 KHz and phase margin as 60° is achieved.

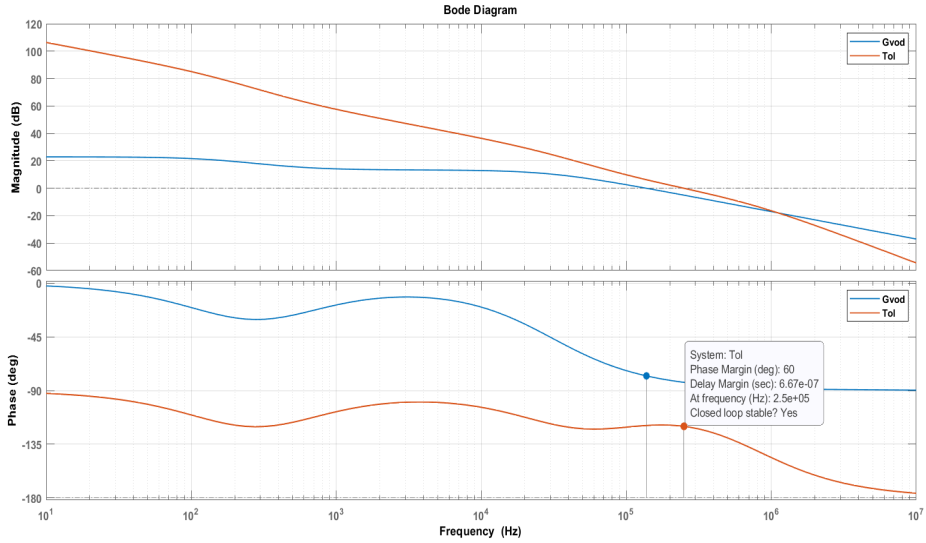


Figure 6.5: Bode plot

Type 2 compensator is equivalent to a PI compensator with an additional high-frequency pole. The purpose of this high-frequency is to force the gain roll-off at high frequencies, beyond the crossover point. It helps to build a good gain margin but also ensures noise immunity by filtering high-frequency spurious noises. By equating equations in 6.46 a relation is obtained between the pole-zero location and the PI coefficients:

$$\tau_i = \frac{1}{w_z}; K_p = w_{p_0}\tau_i; K_i = \frac{K_p}{\tau_i} \tag{6.54}$$

$$PI = K_p + \frac{K_i}{s} \tag{6.55}$$

where, $K_p = 1.8$ and $K_i = 9e05$. A derivative block with coefficient K_d value (1e-10) is used with the above derived PI controller to decrease overshoot. This has negligible effect on the frequency response and stability of the system.

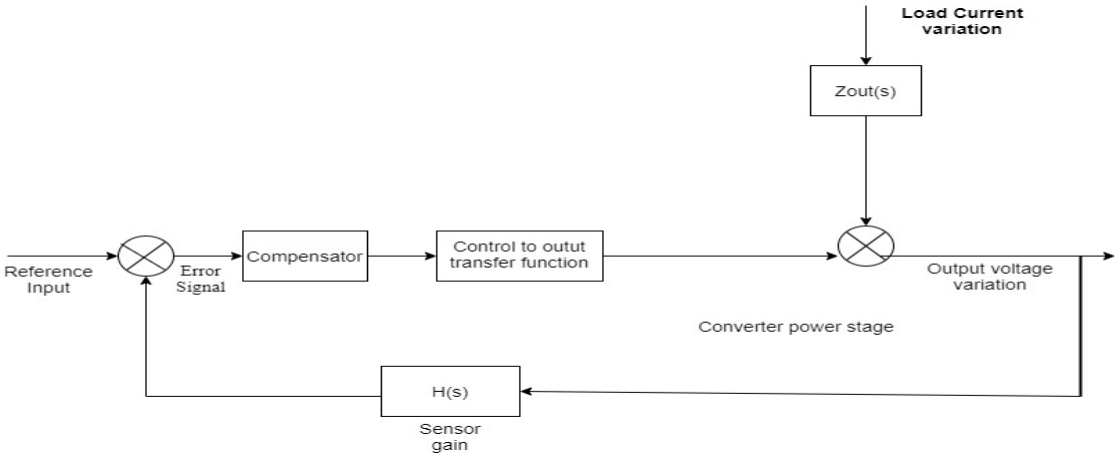
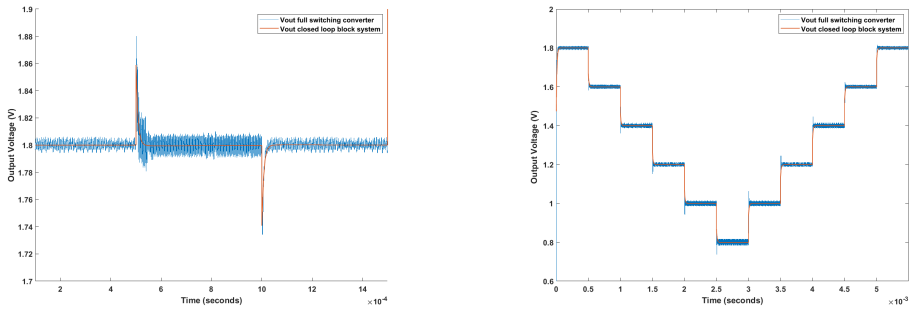


Figure 6.6: Feedback loop system to regulate output voltage

A 50W single DAB converter and a 100W ISOP system including two DAB converters are built in MATLAB/Simulink to verify the analysis and design, with parameters given in table 6.1. A feedback loop block-based system shown in Fig. 6.6 is designed in SIMULINK. To ensure that the small-signal modeling has led us to the correct transfer function, the block system's output voltage response is compared to the output voltage response of the full switching DAB converter. Fig. 6.7(a)

shows the output voltage response in case of the set point (V_{ref}) variation. It can be inferred that the two output voltage waveforms match thus supporting the small-signal derivation. Fig. 6.7(b) shows that the closed loop system is able to regulate and stablizie the output voltage for load transients at 0.5 ms and 1 ms. The above results conclude that the closed loop DAB converter system is stable, and the compensator designed is able to restore system behavior in case of transients.



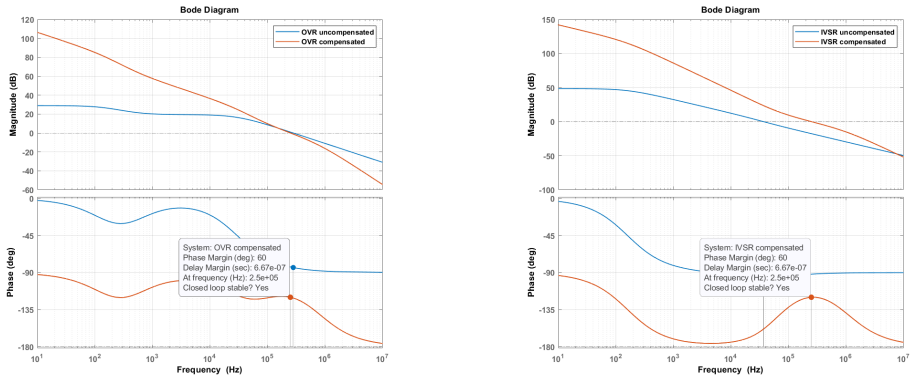
(a) (b)

Figure 6.7: DAB converter output voltage response (a) V_{ref} variation (b) load transient

6.2.2 ISOP system

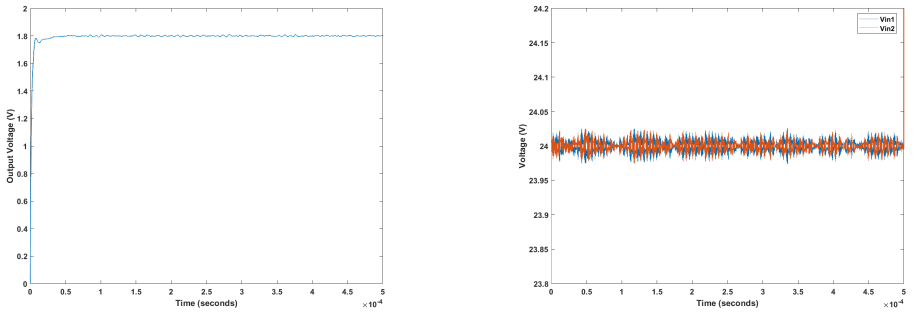
In this subsection the multi-objective controller design for the two DAB module ISOP converter is discussed. The decoupled loop network derived in the previous section enables us to convert this MIMO system into two SISO system and design IVSR loop and OVR independently. The loop gain of output voltage control loop and input voltage sharing control loop are found from Fig 6.2. Compensator design for the following loops is done using the poles and zeros placement method discussed above. The crossover frequency is chosen to be 250kHz which is one-twelfth of the switching frequency. The uncompensated and compensated IVSR and OVR loop gains are shown in Fig 6.8. Through compensation both phase margin and magnitude margin are improved resulting in a stable and fast closed loop system.

Fig 6.9 shows the simulink waveforms for the ISOP converter at full load. It can be observed that the input voltage is evenly shared between the two DAB modules and the output voltage is maintained at 1.8V. In order to verify the performance of the control scheme for an ISOP system, with unmatched modules, the main inductor value for the second converter is altered from 103 µH to 113 µH, all other parameters are same as shown in table 6.1. Fig 6.10 shows the ISOP converter waveforms corresponding to load transient at 0.5 ms and 1 ms. Fig 6.10(a) shows the output voltage of the ISOP during load stepping is regulated and stable. Fig 6.10(b) verifies the operation of the IVSR loop as the input voltage is evenly shared among the two DAB modules. The input voltage for the given ISOP system is stepped



(a) (b)

Figure 6.8: Uncompensated and compensated loop gains in an ISOP system. (a) OVR loop (b)IVSR loop

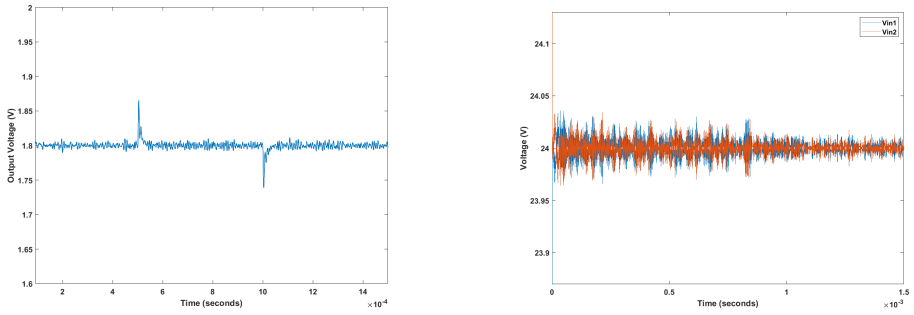


(a) (b)

Figure 6.9: two DAB ISOP system waveforms at full load (a) ISOP system's output voltage (b) Individual module input voltage response

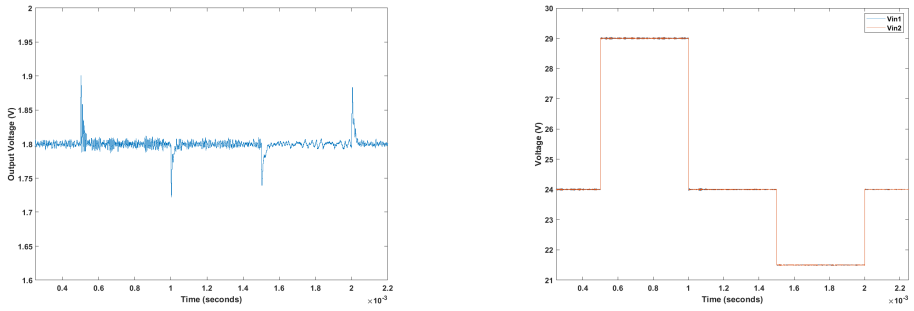
from 48V to 58V at 0.5 ms and brought back to 48V at 1 ms, again stepped down to 43V at 1.5 ms and restored back at 2 ms, the simulink results are shown in Fig. 6.11. Equal voltage sharing is observed among the modules even though they don't have same circuit parameters, this verifies that the control scheme works under input voltage transients and successfully achieves input voltage sharing and output current sharing. The ISOP system is also tested with a new set of control parameter. The new control paramteres are obtained by slightly altering the calculated control parameters.

Fig 6.12 compares the system response to input voltage perturbation with three different set of control parameters. Set1 consists of the calculated control parameters, set2 uses same OVR control parameters as set1 but different IVSR control parameters, and set3 has same IVSR control parameters as set1 but different OVR control parameters. Fig 6.12(a) and (b) represent the system output voltage and module one input voltage for 3 different control parameter sets.It can be observed that as set 2 has same OVR control parameter but different IVSR control parameters than set1, the output voltage response for the two sets is almost same but input voltage differs. Similarly, as set 3 has same IVSR control parameter but different OVR control parameters than set1, the input voltage response for the two sets is almost same but output voltage differs. This verifies that the IVSR and OVR loops are turely decoupled in nature. The closed loop ISOP system is also verified for V_{ref} variations. The results are shown in Fig 6.13.



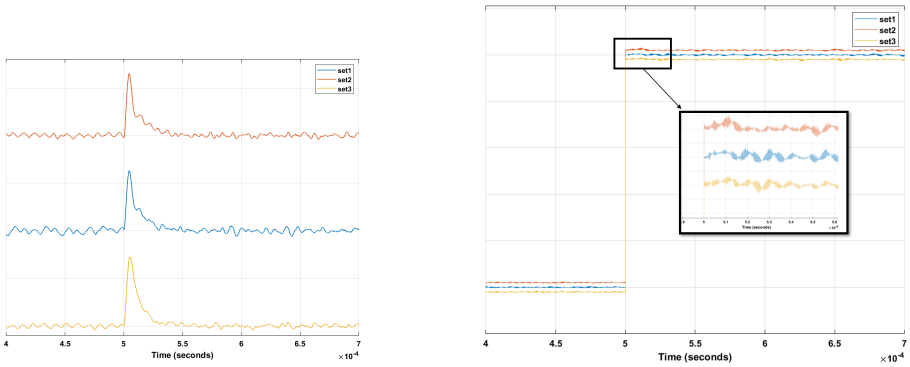
(a) (b)

Figure 6.10: ISOP system waveforms during load transient (a) Output voltage (b) Individual module input voltage



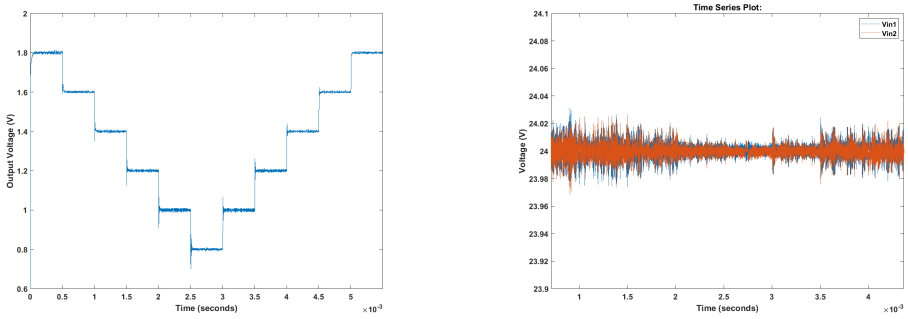
(a) (b)

Figure 6.11: ISOP system waveforms during V_{in} variations (a) Output voltage (b) Individual module input voltage



(a) (b)

Figure 6.12: ISOP system waveforms during V_{in} variations using 3 different set of control parameters (a) Output voltage (b) Individual module input voltage



(a) (b)

Figure 6.13: ISOP system waveforms during V_{ref} variations (a) Output voltage (b) Individual module input voltage

Chapter 7

Results

7.1 Simulation Results

The converter designed is simulated in LTSpice to test the design and verify the calculated parameters and working conditions. The proposed converter is tested at 3MHz switching frequency. The initial sim is shown in the figure below 7.1 which is the single stage DAB converter with one of the branch simulated, with an input voltage of 24V and the switches are driven with ideal gate signals. The results of the sim are shown in the figure below 7.2. From the sim it is shows the basic working of the DAB converter, we can see the trapezoidal behaviour of the main power transfer inductor current, $IL_{main}(A)$ and the square wave pulses of the vh_1 and vh_2 as explained in the chapter 2.

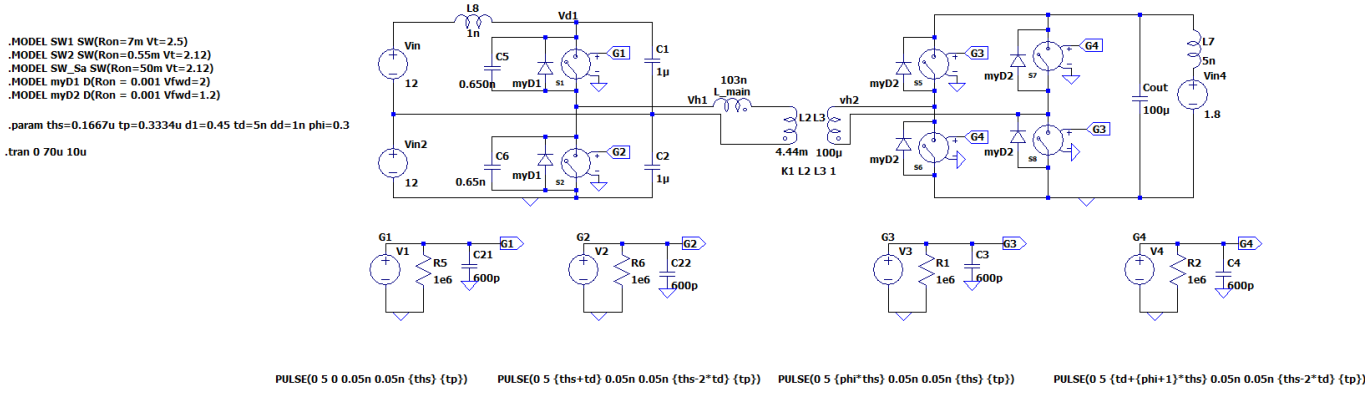


Figure 7.1: Single stage DAB converter

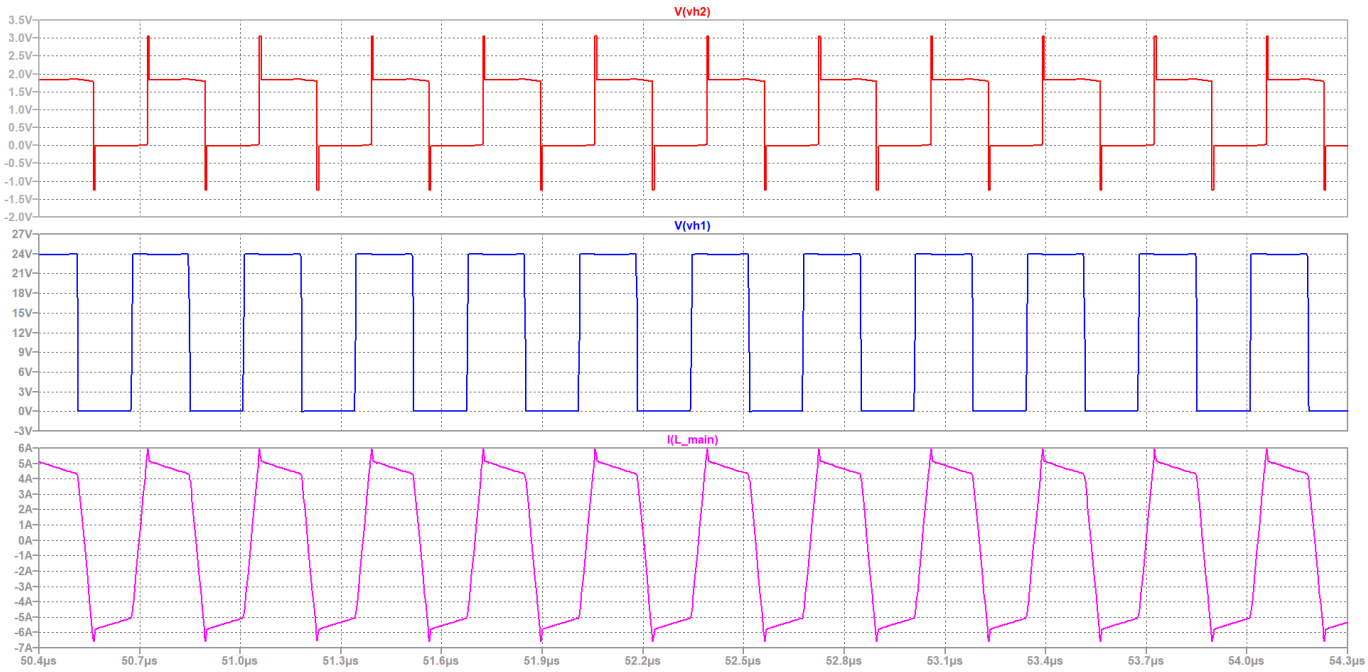


Figure 7.2: Simulation results of single stage DAB converter

The next simulation is the architecture topology proposed for the 48:1.8V conversion, the Input-series-Output-Parallel (ISOP) topology implemented as shown in the figure below 7.3. The two branches are identical to each other and the input is in series and the output is paralleled. This topology selection is explained in detail in chapter 2 in section 2.4. This is again simulated with ideal gate drivers with the phase shift incorporated in the simulations. The simulation results of this sim are shown in the figure below 7.4. The gate driver designs and simulations are discussed later this section.

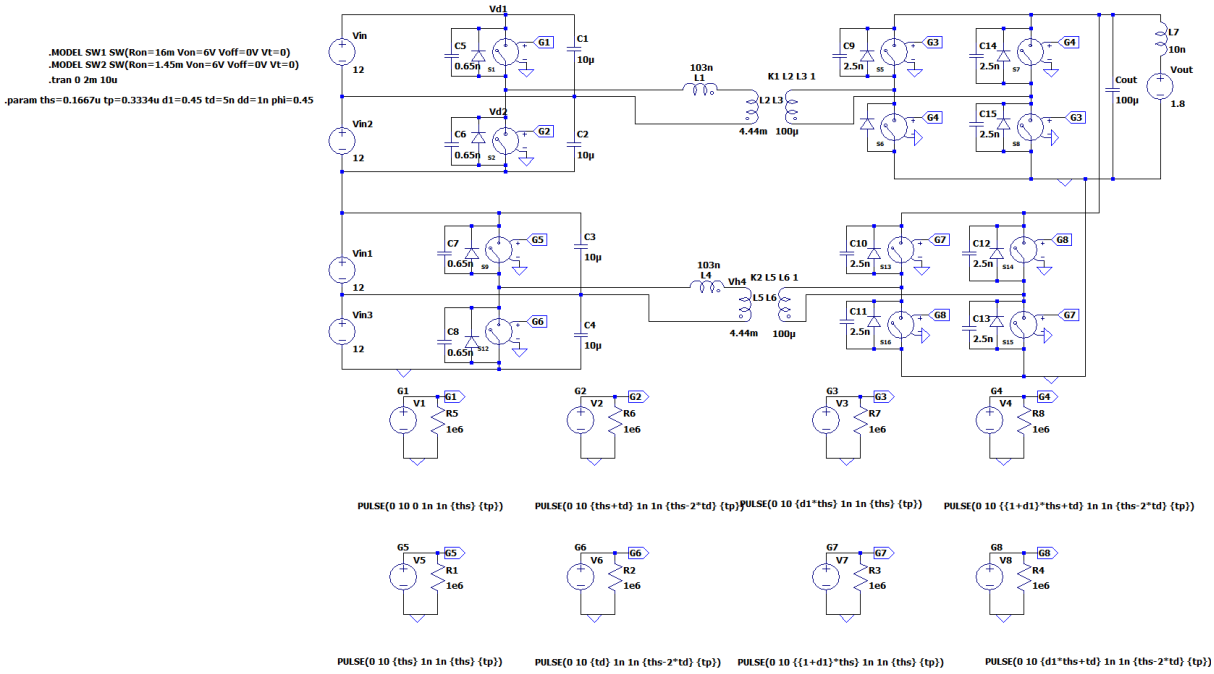


Figure 7.3: Proposed ISOP DAB converter

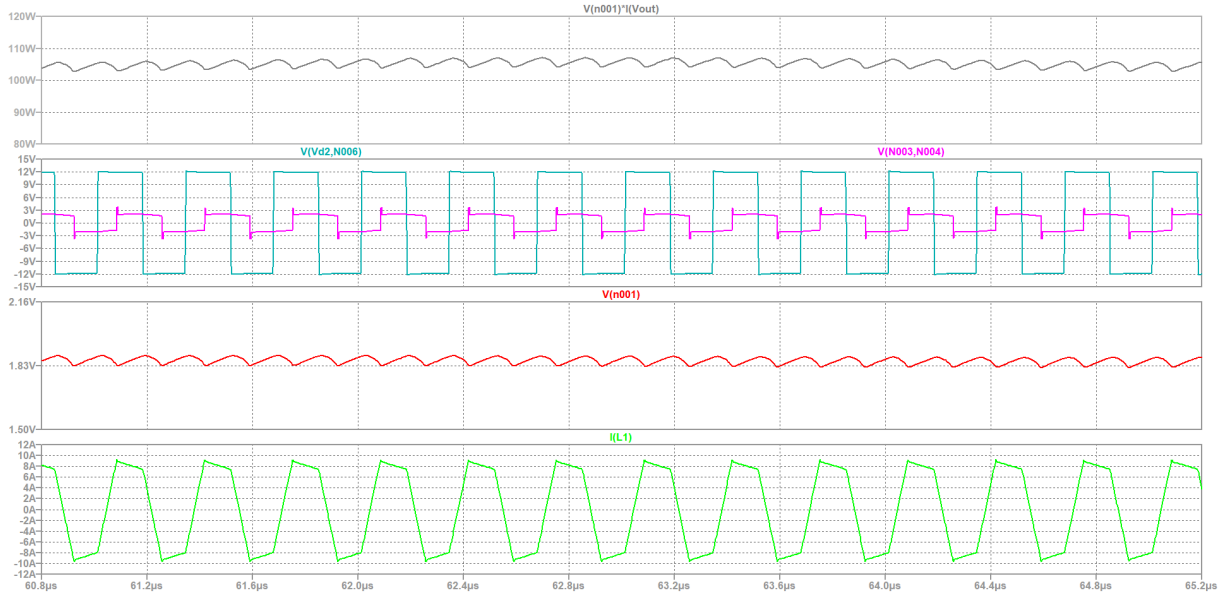


Figure 7.4: Proposed ISOP DAB converter results

From the figure above 7.4 we can see the switching node voltages v_{h1} and v_{h2} are square voltages at the input and the output voltage levels, i.e, 12V and 1.8V. We see 12V on the lower branch switching node because of the half-bridge topology of the converter. We can also see the output power plotted along with the output voltage in open loop control at 1.83V. The main power transfer leakage inductance current plotted has the more-trapezoidal wavelike structure as expected for the DAB converter because of the square wave switching node voltages across the inductor.

The two resonant gate drivers that are discussed and designed in chapter 4 are simulated and tested. The half-bridge gate driver explained in section 4.1 is tested and simulated.The figure 7.5 is the designed resonant gate driver. The half-bridge switches are driven with duty cycle of 50% and then passed through the multi-resonant network. From the equations 4.7 and 4.8 we derived the parameters for the design of the gate driver based upon the impedance analyzer as shown in the figure 4.2 and now simulation also is done with a bit of tuning as shown in the figure below 7.6. After proper tuning of the multi-resonant tank the transient analysis is simulated to verify the output gate voltage waveforms and the results are shown in 7.7.

$$L_f = 182nH, L_{MR} = 85nH, C_{MR} = 5nF \tag{7.1}$$

The output shows that the gate voltages are in fact trapezoidal in shape as expected and thus help reduce the losses in the overall converter.

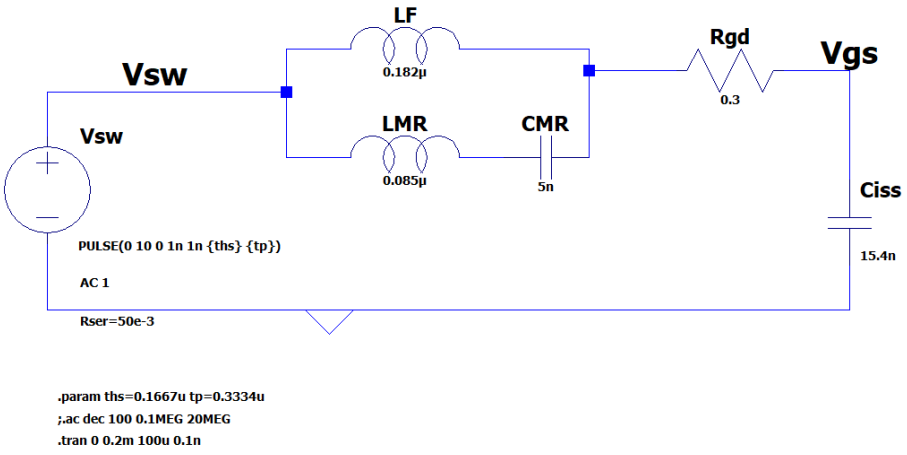


Figure 7.5: Half-Bridge gate driver simulation

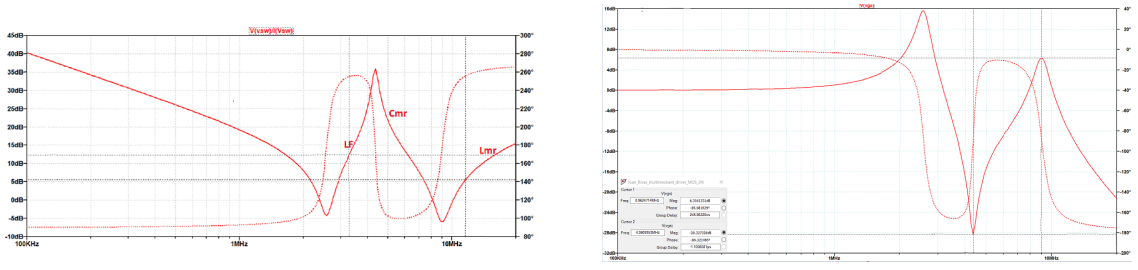
The proposed gate driver for the converter designed is the phi-2 resonant gate driver that is explained in detail in section 4.2 in chapter 4 is tested and simulated for the expected gate voltages.This is a single-switch low side switch gate driver. The parameters are designed according to the equations 4.21 and 4.22.

$$L_f = 50nH, L_{MR} = 500nH, C_{MR} = 1.38nF \tag{7.2}$$

This gives us the schematic as shown in the figure below 7.8. The series inductor L_f we can see that it helps achieve soft-gating by interacting with the C_{iss} of the main power switch and the L_{mr} and C_{mr} resonate at 2^{nd} harmonic frequency and thus we see the more-trapezoidal-like V_{gs} as can be seen in the results in the figure below 7.9.

From the figure it is clear that the power switch is turned on when the gate driver switch is OFF as that is when the input and the inductor L_f is connected to the powerFET. The actual gate voltage od the powerFET M_{main} and the gate signal of the gate driver GaN FET M_D are shown in the figure 7.9. So the power transistor input capacitance C_{iss} is charged/discharged when the switch M_D is turned OFF. A quick transition time is observed and this indicated that high-switching speed is achieved. We can also observe that the powerFET $V(v_{gs})$ comes back all the way to zero before the $V(V_{gsM})$ gate signal of the gate driver GaNFET, M_D is turned on which ensures ZVS switching in the gate driver switch. The performance of this new gate driver proves many more features than a conventional design has.

Now, next step in the simulation is incorporating the proposed gate driver into the converter gate signals and then running the converter with load. This



(a) (b)

Figure 7.6: Half-bridge frequency response analysis (a) Input impedance (b) Output gate voltage

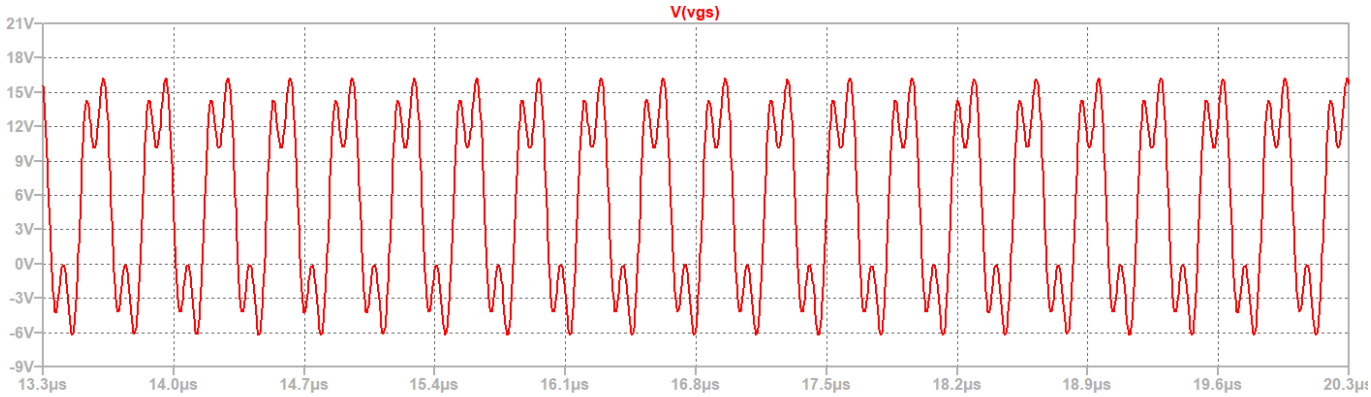


Figure 7.7: Half-bridge output gate voltage

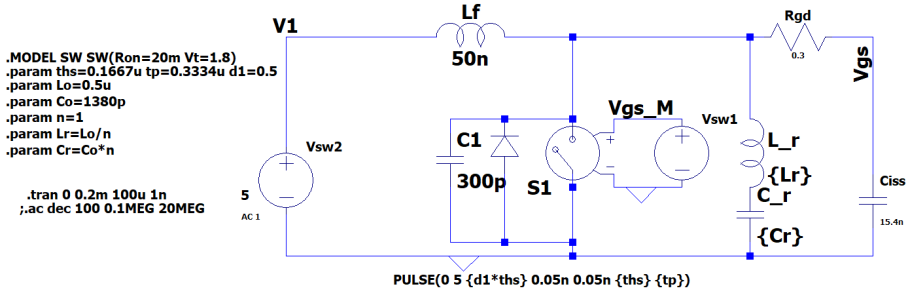


Figure 7.8: Phi-2 gate driver simulation

schematic is shown in the figure below 7.10. The primary is still driven with ideal gate driver voltages, as this is a good enough emulation to the gate driver output of the hardware implementation of the gate driver MCP14700. The dual input synchronous gate driver is very accurate and implement the gate driver signals very close to the pwm signals with a slight delay. The secondary switches are driven with the phi-2 gate drivers. Here we can see that 2 switches are driven with a single phi-2 implementation, since the C_{iss} of one switch of TPWR6003PL, mosfet selected for the secondary switch is 7.7 nF, here the phi-2 is simulated with a C_{iss} of 15.4 nF. The simulation results of this simulation are shown in the figure below 7.11.

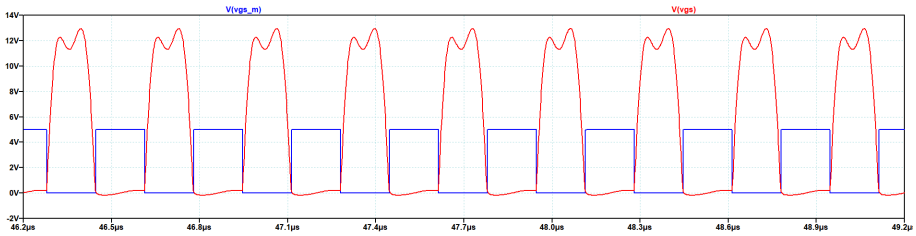


Figure 7.9: Phi-2 gate driver output gate voltage

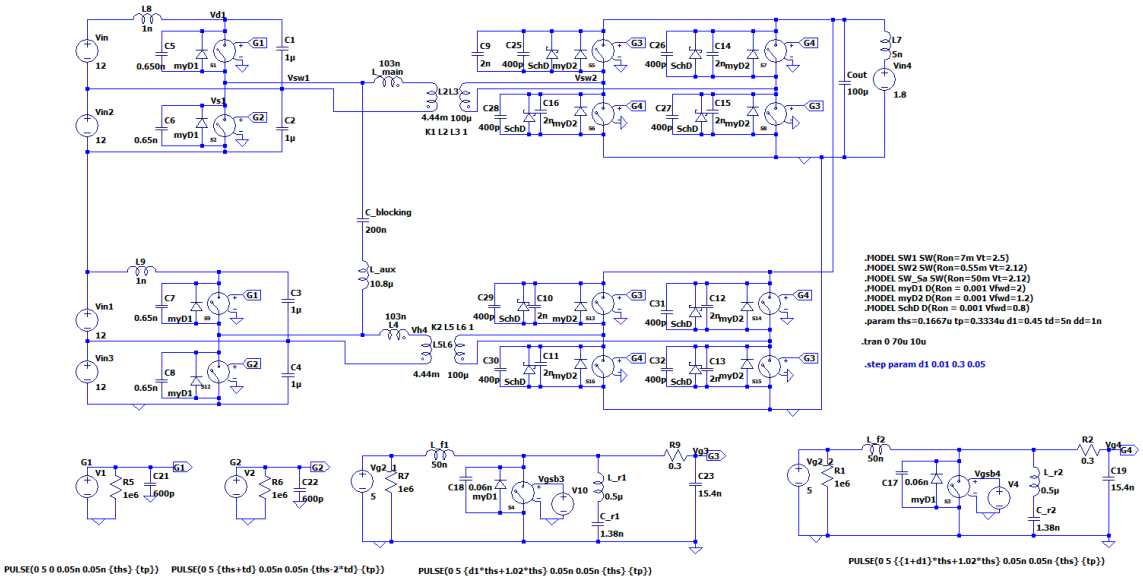


Figure 7.10: Complete converter simulation with the Phi-2 resonant gate drivers

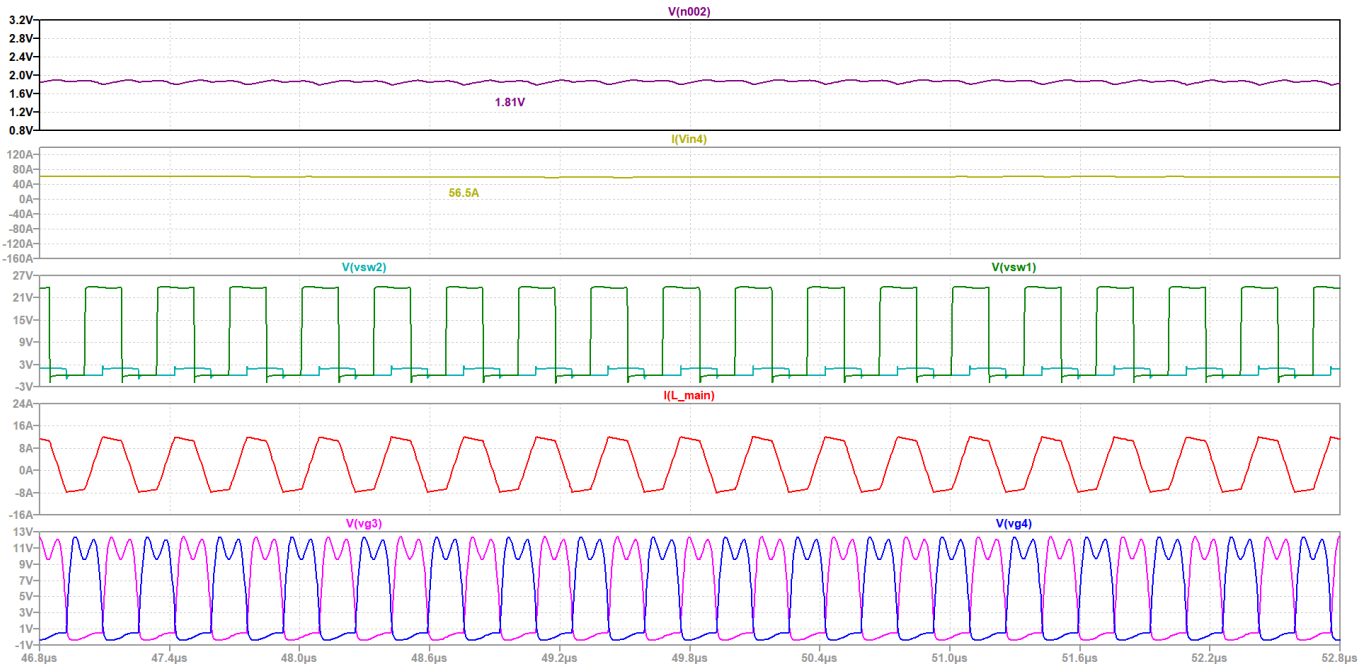


Figure 7.11: Sim results of the converter with the Phi-2 resonant gate drivers

From the simulation results shown above figure 7.11 we can observe the gate signals of the full-bridge of the secondary side, V_{gs3} and V_{gs4} which can be seen from the figure that they are trapezoidal as expected and are at 12V max voltage so that we could ensure that the Si switches of the secondary are completely turned ON with as minimum R_{dson} as possible. The output voltage and current of the converter are plotted and this is at full load and thus the light load auxiliary inductance doesn't have any role to play here. The switch node voltages, $V(V_{sw1})$ and $V(V_{sw2})$ of the low side branch of the converter are also plotted which are 24V square wave and the 1.8V on the primary and secondary side switching node respectively as expected and thus the inductor current across the main power transfer inductor is trapezoidal as expected at full-load conditions.

7.2 Experimental Results

The figure below shows figure 7.12 the converter after the pcb layout in KiCAD and fabricated. The PWM signals are plotted in the figure shown below

7.13. The pwm signals shown in the figure below are for the primary and the secondary branches, and we can observe the 30° phase shift between the primary pwm signal, V_{g1} and secondary signal, V_{g3}.

Figure 7.12: Converter board

The primary half bridge is then tested next for the working of the primary GaN switches, GS61008T and the primary gate drivers, MCP14700. The figure

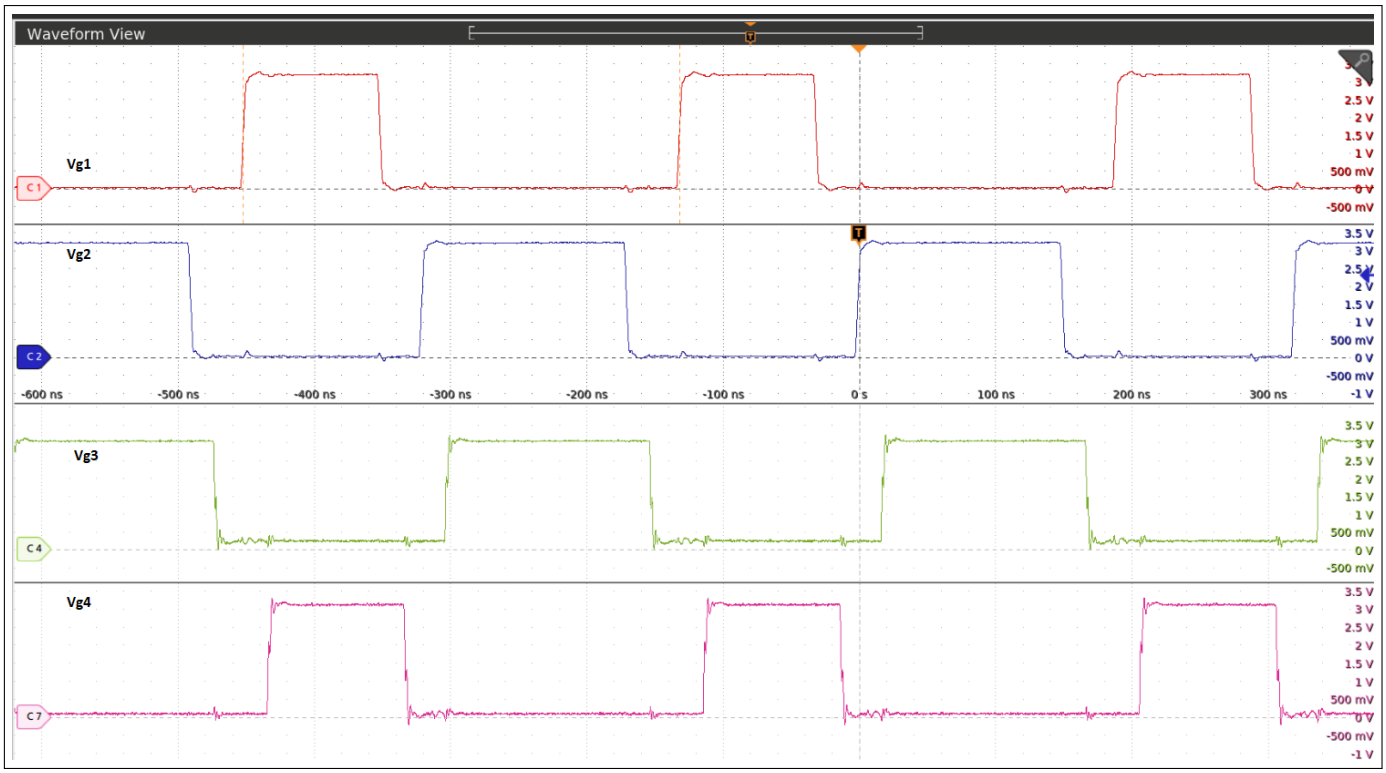


Figure 7.13: PWM signals for one branch of the converter

below 7.14 shows the drain and gate voltages of the low-side primary switches.

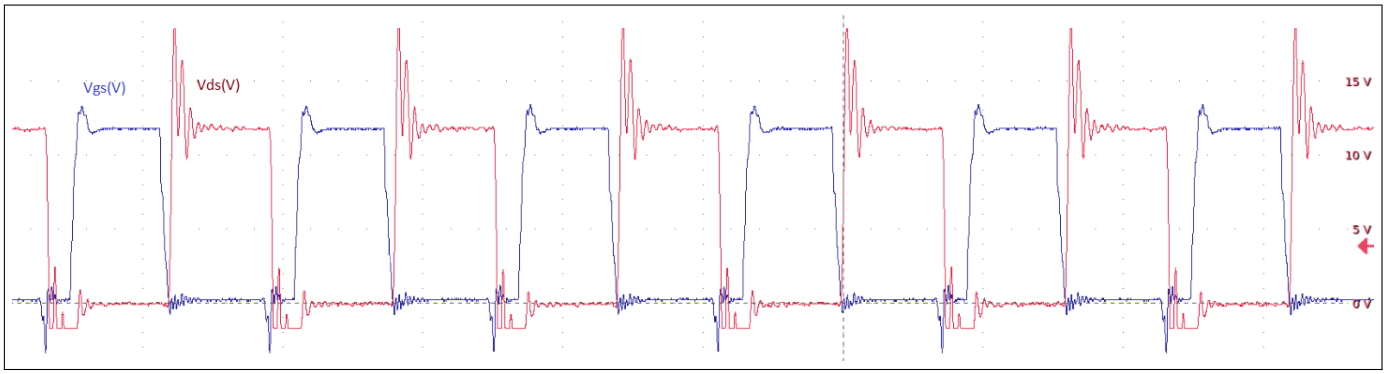


Figure 7.14: Drain and gate voltages of the primary bridge

From the figure above 7.14 we can observe that we achieve soft-switching ZVS as the drain voltage comes down to zero before the gate voltage is given and

we can even see some body diode conduction and thus there is some body diode losses in the primary switches, better tuning of the deadtime we could avoid this body diode losses too.

The first important module to test in the secondary side is the phi-2 resonant gate driver to get it to working to drive the secondary MOSFETs. The secondary switches TPWR6003PL are placed for the test at the high side and low side for the V_{g3-Ls} and V_{g3-Hs} and the L_f, L_{mr} and C_{mr} are placed according to the parameters in the equation 7.2 as shown in the figure below 7.15.

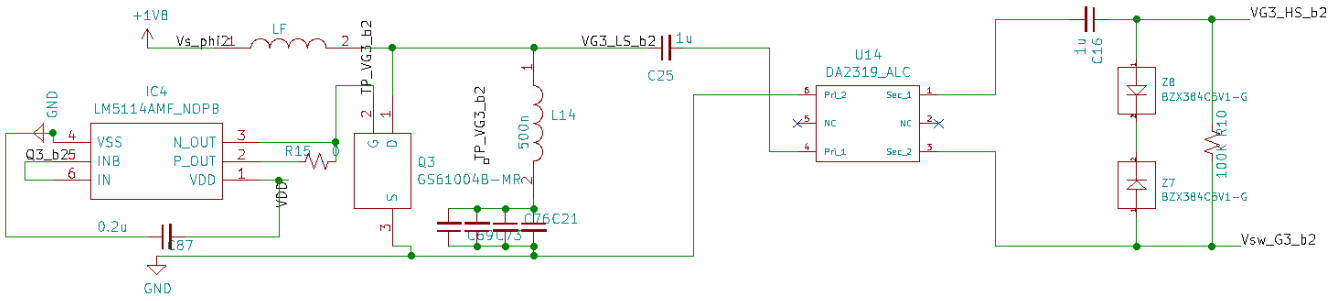


Figure 7.15: Phi-2 resonant converter experimental schematic

The Phi-2 gate driver switch is the GaN switch GS61004B and is driven by the low side gate driver LM5114. The 1:1 transformer is put to have isolation of the grounds of the gate signals for the high-side and low-side switches which would be switching node and the ground signals. With this setup in place, there needed a lot of tuning in order to get the waveform as expected.

$$L_f = 45nH, L_{MR} = 500nH, C_{MR} = 5nF \tag{7.3}$$

The results are shown in the figure below 7.16. But this is not valid as there was a major artifact involved in the tuning of this gate driver which was missing in the simulation, the leakage inductance of the 1:1 transformer. The transformer in place. DA2319ALC in the setup has a leakage inductance of 1.5 μH, which when in series with the C_{mr} and C_{iss} acts as a perfect filter and resonate very close to the second harmonic frequency of the gate driver and thus filters out the high-side voltage.

This could be rectified by few measures: (1) Re-design the 1:1 transformer with much lesser leakage inductance, ideally less than 10 nH (2) Short the high

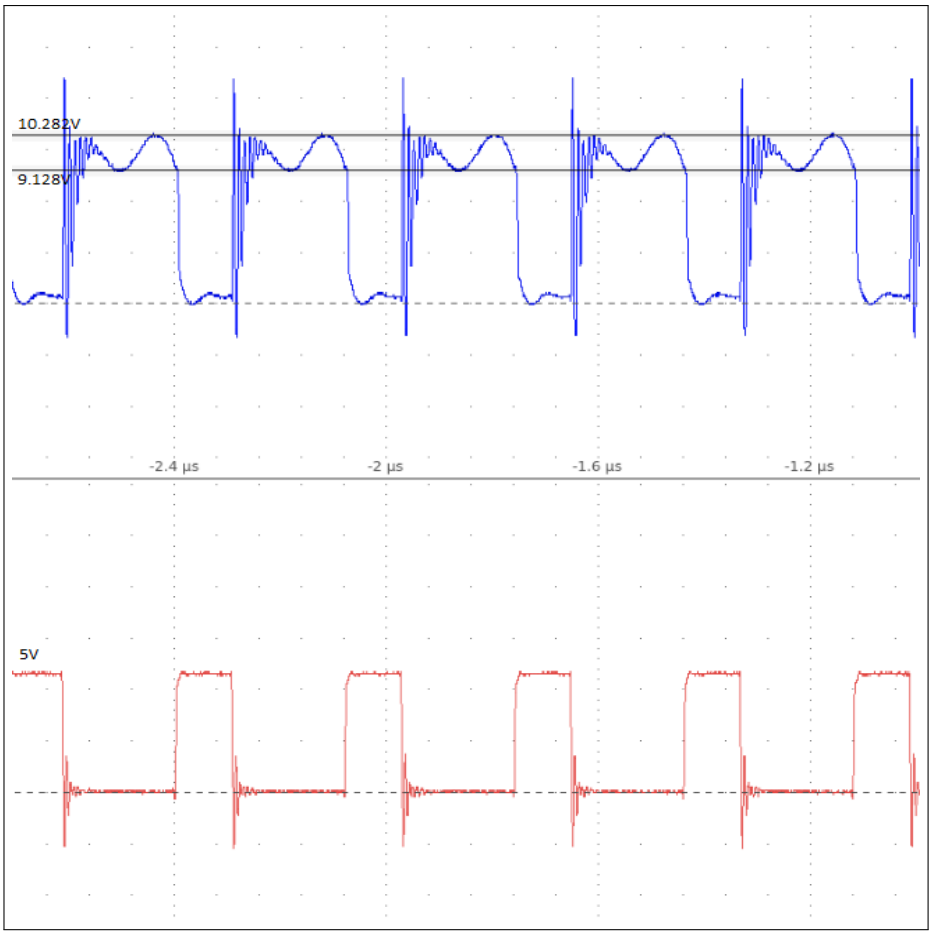


Figure 7.16: Phi-2 resonant converter results

and low side gate drive signals, since the Si switches are completely turned on at 10V, instead running both these at 12V would allow the high side gate signal to have a V_{gs} of 10V since the output voltage is 1.8V in this specific application. (3) Better solution would be to re-design the high-side and low-side gate drivers to have independent phi-2 gate drivers so that the tuning wouldn't impact each other.

The first method was applied and the 1:1 transformer was re-designed with the available cores. The figure below 7.17 shows the pic of the designed transformer, with 50 nH leakage inductance and 30 μH magnetizing inductance with 80-toroid Ferrite cores. But the simulations were not good enough high-side voltages, even with having a dc-blocking capacitor and a diode between the gate and source in-order

to restore the dc voltage of the gate signals after passing through the transformer, the voltages as seen from the figure below 7.18 the high-side waveforms are still very distorted.

Figure 7.17: 1:1 xfmr with lower leakage

Thus, the second method is applied where the primary and secondary are shorted and then 12V of V_{gs} is driven so that the high-side could still get 10V for it to turn on at 1.8V output voltage. This is then tested with the complete one branch of the DAB converter working. The figure below 7.19 shows the results.

From the below figure 7.19 we can see that there is overlap between the gate voltages which is dangerous as there needs to be a deadtime and thus avoid shoot-through of the secondary switches. Thus, the pwm signals need to have negative dead-time inorder for the gate signals to actually have some positive deadtimes. The results are shown in the figure below 7.20. But there needs to be further tuning of the micro-controller to allow ZVS switching of the GaN switches and thus avoid

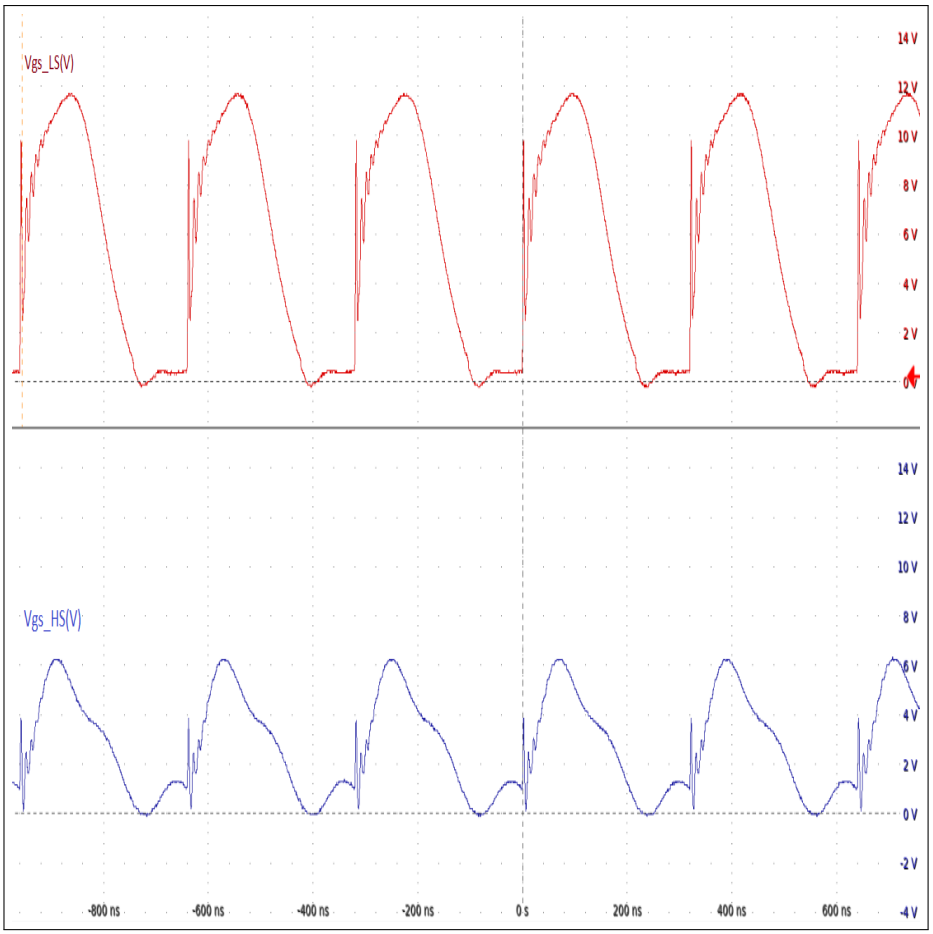


Figure 7.18: Low side and high side voltages of the gate signals with the new transformer

additional losses.

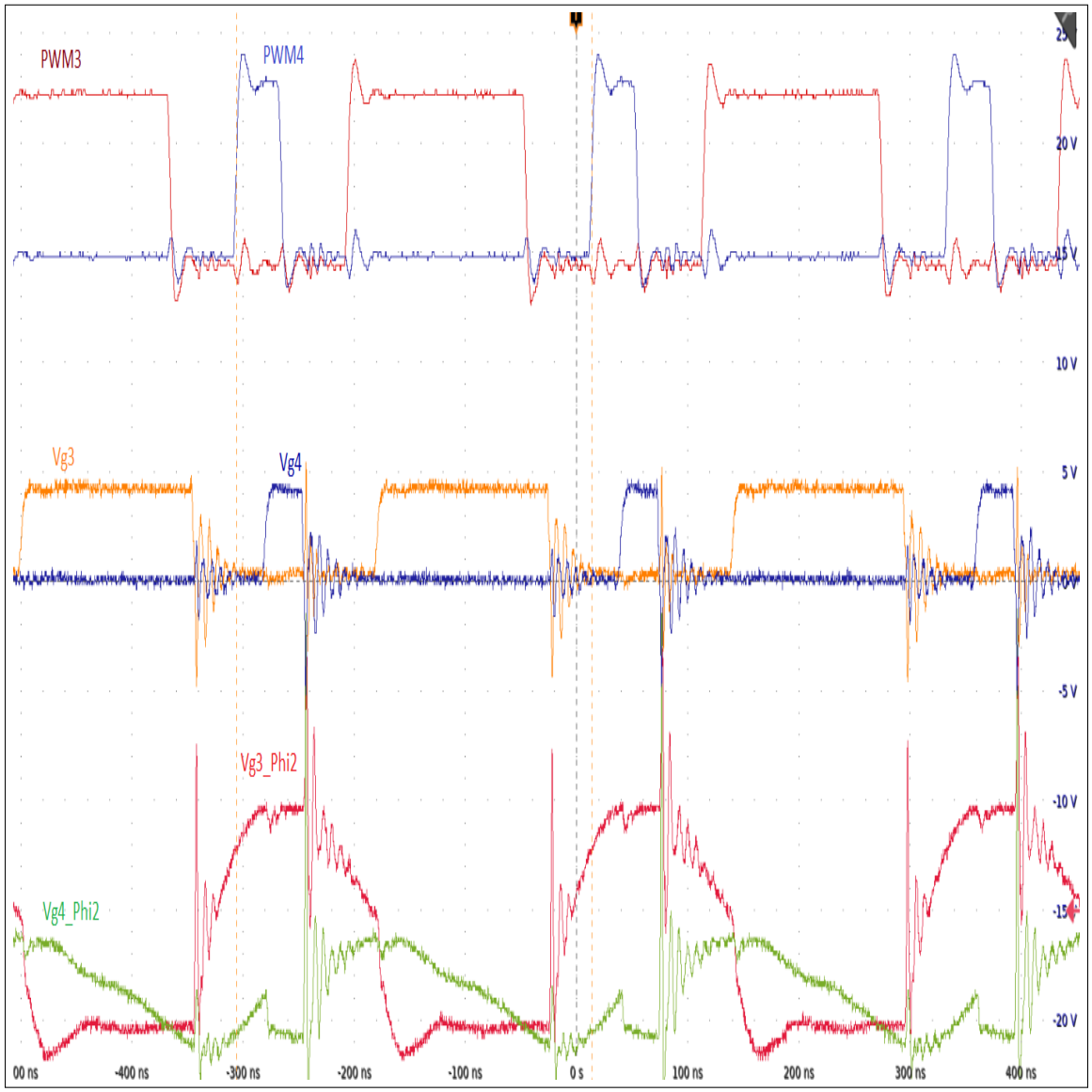


Figure 7.19: Phi-2 gate driver results output without deadtime

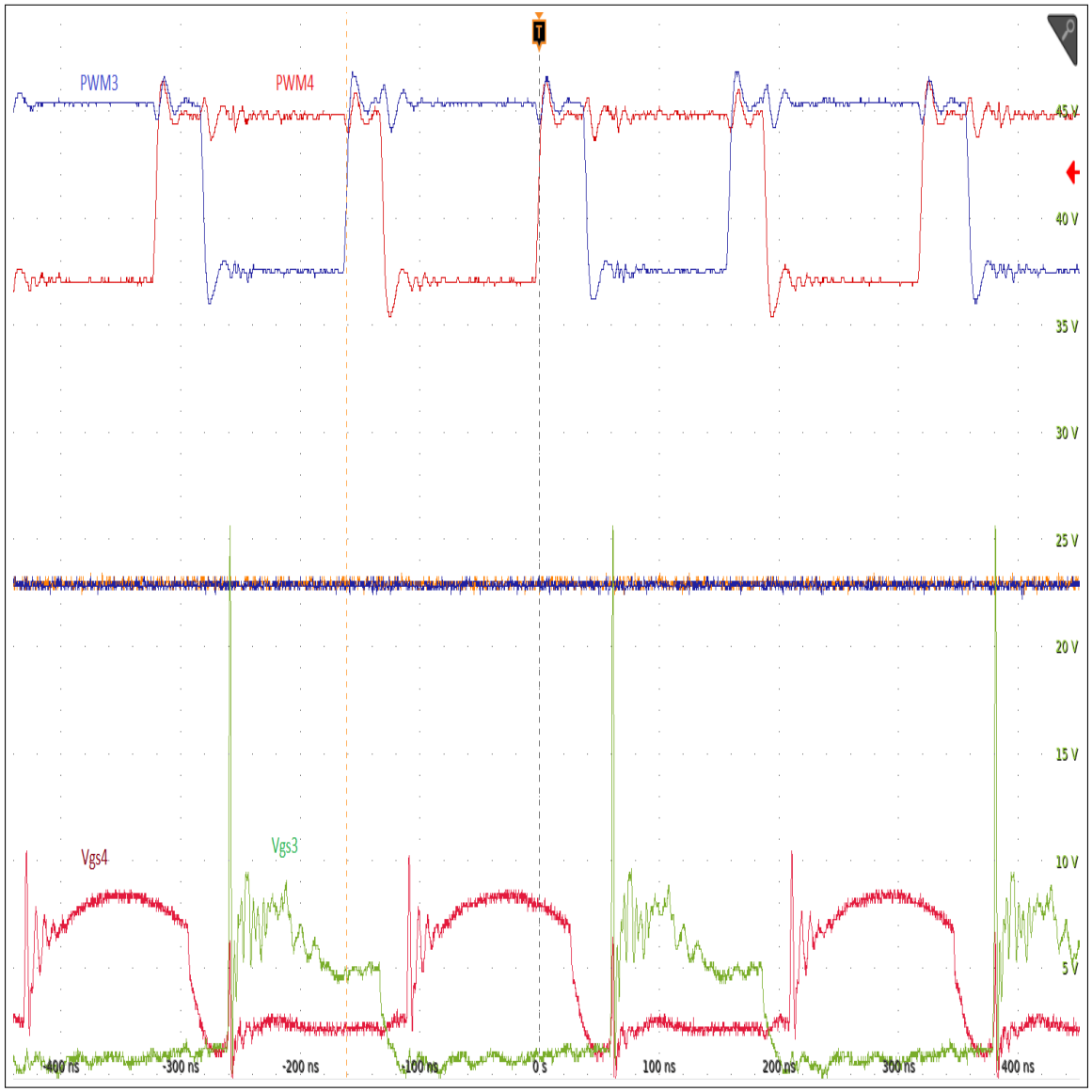


Figure 7.20: Phi-2 gate driver results output with deadtime

Chapter 8

Conclusions

This Thesis work was focused on explaining detailed design guidelines of high conversion ratio single-conversion stage Dual Active Bridge converter. The results from the simulations show that DAB converter outperforms the conventional converters in number of different factors such as bi-directional conduction, lower losses due to easy ZVS soft switching in all the switches and higher conversion ratio due to the transformer turns ratio and many more which are mentioned in detail in the chapters in this work.

The following topics have been discussed in this Thesis work. The main characteristics for Chapter 2 Design procedure of DAB converter and the parameter selection through data driven analysis, Chapter 3 the light load efficiency improvement technique without impacting the full-load efficiency, and Chapter 4 the single-switch ZVS gate driver based on the class ϕ-2 resonant gate driver are:

- The steady state waveforms are explained and analyzed in detail
- The expressions for the parameter design and solution derivation have been explained
- The gate drivers are simulated and tested on LTSpice and the tuning process with design principles is presented.

From the simulation results we can understand the design of a Dual-Active bridge converter and also a resonant gate driver analysis and design. Unfortunately, due to delay in arrival of the pcb board and the GaN switches being unavailable or out of stock has delayed the experimental results and thus not able to have many experimental results. But my observations from the experimental results were: (1) It is definitely encouraged to design the low-side and the high-side to have separate ϕ-2 gate drivers as the isolation transformer will add in a lot of unwanted behaviour through the leakage inductance of the transformer and thus undauntedly creating another ϕ-2 with the high-side gate voltage output signal.

8.1 Future Work

To re-design the ϕ-2 gate driver with the low-side and high-side gate driver separately tuned and then tally the losses individually. This could also include having a single ϕ-2 but to have very minimal leakage inductance or to have a wide-band inductance canceller network inorder to cancel the impact of leakage inductance of the transformer atleast to the order of 5^th harmonics. To experimentally prove the soft-gating and the light-load efficiency improvements as explained in the simulations.

Chapter 9

Appendix A

9.1 Dual Active Bridge Parameters derivation Analysis Code

Table of Contents

Calculation of Tdead_min and primary switch Ron and frequency

```
P_FL = 50; %Each converter in parallel would be 50W contributed
Vin = 24; %Each converter is 24V
Vout = 1.8;
fsw = 3e6; %Frequency set is 3MHz
Ths = 1/(2*fsw);
D_FL = 0.45; % Full load at the maximum allowable phase shift ratio
N = 0.5*Vin/(Vout); % Turns ratio, 0.5Vin due to half bridge in
 primary
L_FL = ((1-D_FL)*D_FL*Ths*(N*Vout)^2)/(P_FL);
IL_FL_pk = (Vin*0.5*D_FL*Ths)/(L_FL); %Assuming matching case
 Vin=NVout

%Full load deadtime for min ZVS calculation on primary
Coss = 1500e-12;
Ron = linspace(1e-3,10e-3,100);
FOM = 4e-12;%Considering 4mohms and 1500pF
T_dead = (2*Vin*FOM/IL_FL_pk)./Ron;
T_dead_per = T_dead*fsw;
plot(Ron,T_dead_per);
hold on

%Primary Conduction loss calcuation
ILrms_FL = IL_FL_pk/sqrt(2); %Assumption (if inductive load)
P_cond = 2*(ILrms_FL^2).*Ron; %Conduction loss in one converter (2
 devices)
P_cond_per = P_cond/(P_FL);
plot(Ron,P_cond_per);
legend('T dead/T','P-cond/P-FL');
xlabel('Ron');
%ylim([-0.5e-3 1.5e-3])
hold off
```

Calculation of Tdead_new and aux inductance and blocking cap

```
%Diode loss calcuation
T_dead_1 = 6.5e-9; %Result from sim, handcal 7.5e-9
```

```
Ron_1 = 7e-3; %7mohms is the Ron of GS61008T
Coss_1 = 650e-12; %650pF is the Coss of GS61008T
FOM_1 = Coss_1*Ron_1;
Vf_drop = 2; %Assumption
T_dead_new = linspace(1e-9,30e-9,500);
Q_aux = 200; %Assumption of Q=WL/R to start with
P_diode = (((2*Vf_drop*IL_FL_pk).*(T_dead_new))-
((2*Vf_drop*ILrms_FL)*T_dead_1))*(fsw);
P_diode_per = P_diode/P_FL;
figure
plot(T_dead_new,P_diode_per);
legend('P-diode/P-FL');
xlabel('T dead new');

%Switching loss calcuation
P_sw = 2*Coss_1*(Vin)^2*fsw;
%Conduction loss at light load calcuation
D_LL = 0.05; %light load duty cycle
Ipk_aux = (2 *Coss_1*Vin)./T_dead_new;
L_aux = (Vin*(1-D_LL)*Ths)./Ipk_aux-(Vin.*T_dead_new)./Ipk_aux;
C_aux = (50/(((2*pi*fsw)^2)))./L_aux;
Irms_aux = Ipk_aux/sqrt(3); %triangle wave rms=pk/sqrt(3)
P_cond_light_sw = 2*(Irms_aux).^2*Ron_1;
R_aux = (2*pi*fsw/Q_aux).*L_aux;
P_cond_Raux = (((Irms_aux).^2).*R_aux);
P_cond_light_total = P_cond_light_sw + P_cond_Raux;
P_cond_light_per = P_cond_light_total/P_sw;
figure
plot(T_dead_new,P_cond_light_per,'r');
%ylim([-0.5e-2 50e-2])
legend('P-cond light/P-sw');
xlabel('T dead new');
```

Adaptive deadtime control

```
%After looking at the trade off between the diode loss and the
 conduction
%loss we see that just switching at one light load condition isnt
 working
%too much diode loss (GaN devices)

% For smooth operation of DAB without having the deadtime negative
 effects
% M < D/2
%Optimized deadtime as a function of load
Phi_max = 0.1818; %0.055;%%0.1109; %0.1818;% %;%0.02778;%Needs change
 when testing for different Tdead_max
Phi = linspace(0,0.45,100);
M = Phi./2;
figure
plot(Phi,M,'g');
ylim([0 0.1])
hold on
```

```
Phi = linspace(Phi_max,0.45,100);
Ipk_phi = (Vin*0.5*Ths/L_FL).*Phi; %Vin*0.5 since half bridge and
 Vin=NVo
T_dead_phi = (2*Coss_1*Vin)./Ipk_phi;
T_dead_phi_per = T_dead_phi*fsw;
plot(Phi,T_dead_phi_per,'r');
xlabel('Phase shift ratio');
Tdead_max = 0.03/fsw; %Needs change when testing for different
 Tdead_max
%legend('T dead/T');
Ipk_max = 2*Coss_1*Vin /Tdead_max;
L_aux_max = (Vin*(Ths-Tdead_max))/Ipk_max;%Laux would give
%ZVS at no load with Tdead/T = 0.1
Phi = linspace(0,Phi_max,100);
Phi = double(Phi);
syms Td
%Ipk_Daux = ((Vin*0.5*Ths/L_FL).*Phi)+(Vin*(Ths-T_dead_phi_aux)/
L_aux_max);
%T_dead_phi_aux = (2*Coss_1*Vin)./Ipk_Daux;
%eqn = ((Vin*(Ths-Td))/L_aux_max)+((Vin*Phi)/(4*L_FL*fsw)) ==
 (2*Coss_1*Vin/Td);
eqn = (Vin*(Td)^2-(Td*Vin/(2*fsw))*(1+((L_aux_max.*Phi)/
(2*L_FL)))+(2*Coss_1*Vin*L_aux_max))==0;
for i= 1:100
    eqn_1 = eqn(1,i);
    T_dead_phi_aux_1 = vpasolve(eqn_1,Td,[0 Inf]);
    T_dead_phi_aux(i) = T_dead_phi_aux_1(1,1);
end
T_dead_phi_aux_per = T_dead_phi_aux*fsw;
plot(Phi,T_dead_phi_aux_per,'b');
legend('M=Phi/2','T dead/T','T dead aux/T');
hold off

%Pcond/Psw loss at no load with the Laux in place with varying
%Tdead_new_max to see its effect on the losses and decide the T_dead
 max
%
T_dead_max = linspace(0.001e-9,50e-9,100);
T_dead_max_per = T_dead_max*fsw;
Ipk_aux_max = (2 *Coss_1*Vin)./T_dead_max;
L_aux_max = (Vin*(Ths-T_dead_max))./Ipk_aux_max;
Irms_aux_max = Ipk_aux_max/sqrt(3); %triangle wave rms=pk/sqrt(3)
P_cond_noload_aux_sw = 2*(Irms_aux_max).^2*Ron_1;
R_aux_max = (2*pi*fsw/Q_aux).*L_aux_max;
P_cond_Raux_max = (((Irms_aux_max).^2).*R_aux_max);
P_cond_light_aux_total = P_cond_noload_aux_sw + P_cond_Raux_max;
P_cond_light_aux_per = P_cond_light_aux_total/P_sw;
figure
plot(T_dead_max_per,P_cond_light_aux_per,'r');
ylim([0 1])
legend('P-cond aux noload/P-sw');
xlabel('T dead max/T');
```

Secondary switch design

```
%Max deadtime to avoide diode conduction/ Min deadtime to get ZVS at
 FL
Ron_2 = 1.45e-3;%linspace(0.1e-3,4e-3,100);% %1.45e-3 for epc2023 %
FOM_2 = 3.335e-12; %4e-12; %3.335e-12 for epc2023
T_dead_2 = (2*Vout*FOM_2/IL_FL_pk)./Ron_2; %at FL IL = 7.57A,
 Tdead=1.09e-9 for epc2023
T_dead_2_per = fsw.*T_dead_2;
figure
plot(Ron_2,T_dead_2_per);
xlabel('Ron 2');
legend('Tdead/T main sw ZVS');

% Gate inductance calculation for soft gating
Vg = 5; %5V gate voltage epc2023
Rgd = 20e-3; %On resistance of one of the gate driver's switch
Cgs_2 = 2050e-12; % FOM_2./Ron_2;%Assuming that Coss = Cgs % 2050e-12
 for epc2023
Qgate_aux =100; %Assumption
dead_time_factor = 3; %Change continuously to test
T_dead_g = dead_time_factor.*T_dead_2;
syms Lg_aux %= linspace(10e-9,1e-5,10000);
%Lg_aux_1 = (1/(4*fsw)).*T_dead_g;
%Lg_aux = Lg_aux_1./Cgs_2;
%T_dead_g = 3e-9;%(4*Cgs_2*fsw).*Lg_aux;
%RL_aux = ((2*pi*fsw)/Qgate_aux).*Lg_aux;
%T_dead_g_per = fsw.*T_dead_g;
figure
plot(Ron_2,T_dead_g_per);
xlabel('Ron 2');
legend('Tdead gate/T');
%Secondary conduction loss with Aux inductance for soft gating
IL_g_pk = (Vg/(4*fsw))./Lg_aux;
ILrms_g = (1/sqrt(3)).*(IL_g_pk); %Assuming triangle wave
%P_cond_2 = 2.*((ILrms_g).^2).*(2*Rgd+RL_aux); %Conduction loss in one
 converter (2 devices)
P_sw_2 = 2*Cgs_2*(Vg)^2*fsw;
Lg_aux2 = Lg_aux.^2;
Ptotal1 = ((Vg)^2/(48*(fsw)^2))./Lg_aux2;
Ptotal2 = (2*Rgd).*Ptotal1;
Ptotal3 = ((2*pi*fsw)/Qgate_aux).*Ptotal1;
Ptotal31 = Ptotal3.*Lg_aux;
Ptotal4 = Ptotal2+Ptotal31;
Ptotal5 = (T_dead_g/4*fsw*Cgs_2)./Lg_aux;
Ptotal6 = 1- Ptotal5;
Ptotal7 = Ptotal6.^2;
Ptotal8 = 2*Cgs_2*(Vg)^2*fsw.*Ptotal7;
%P_half_gating = 2*Cgs_2*(Vg)^2*fsw.*((1-(T_dead_g./
(4.*Lg_aux*fsw*Cgs_2))).^2);
P_total_2 = Ptotal4 + Ptotal8;
P_cond_total_2_per = (1./P_sw_2).*(P_total_2);
figure
```

```
fplot(P_cond_total_2_per)
%plot(Lg_aux,P_cond_total_2_per);
hold off
legend('P-cond-2/Psw-2');
xlabel('L aux');
% With the plots with Pcond/Psw even with not complete soft gating the
% Pcond loss were much more than expected and thus not beneficial from
% doing soft gating..
%Gate energy
IL_FL_pk_2 = (Vout*D_FL*Ths)/(L_FL);
P_gate_2 = 0.5.*Lgate.*(IL_g_pk.^2);
P_Leak_FL = 0.5*L_FL*(IL_FL_pk_2^2);
P_gate_2_per = (1/P_Leak_FL).*(P_gate_2);
figure
plot(Ron_2,P_gate_2_per);Lg_aux_1
legend('P-gate-2/P-Leak');
hold on
```

Half-Bridge multiresonant gate driver

```
fsw = 3e6;
Vg = 5;
Vg_sa = 5;
j = sqrt(-1);
ws = 2*pi*fsw;
for n1 = 1:8% n1 is the number of GaN switches in parallel
Cgs_2_n(1,n1) = (n1*7480e-12);%7480e-12; for Si FET %n1*(2050e-12) for
 epc2023;
Ciss_2(1,n1) = n1*7700e-12;% 7700e-12;for Si FET %n1*2150e-12 for
 epc2023;
Rgd(1,n1) = (0.6)/n1; %0.6;for Si FET  %(0.3)/n1 for epc2023;
Ron_2_n(1,n1) = (0.55e-3)/n1;%(1.45e-3)/n1; % for Si FET ;%(1.45e-3)/
n1;for epc2023;
R_sa = 50e-3; %Driver Rout around 100mohms and below is better
 variation in soft and hard and soft gets more efficient
FOM_sa = 3.335e-12;
Cgs_sa = FOM_sa/R_sa;
L_f(1,n1) = 1/((ws^2).*Ciss_2(1,n1));
C_mr(1,n1) = Ciss_2(1,n1)*0.37;
L_mr(1,n1) = 1/(((ws*3)^2).*C_mr(1,n1));
%C_mr = 1.911e-9;%2.52e-9; % for Si fet %9.32e-9;%8.4e-9;%7.5e-9;
%6.5e-9;%5.5e-9;%4.5e-9;%3.5e-9;%2.6e-9;%1.811e-9;%0.85e-9;
%vpa(abs(ans)) From the sim with ~1db
%C_mr = 0.955e-9;1.911e-9 for 2 in parallel%2.86e-9 for 3 in
%parallel,3.8e-9 for 4,%4.7e-9 for 5% 5.7e-9 for 6% 6.69e-9 for 7%
 7.64e-9
%for 8% 8.6e-9 for 9% 9.55e-9 for 10
%L_mr = 0.1e-6;%0.22e-6;%for Si fet %0.017e-6;%0.018e-6;%0.02e-6;
%0.029e-6;%0.035e-6;%0.04e-6;%0.06e-6;%0.85e-7;%0.1e-6;%0.73e-6;%From
 the sim with ~1db
%L_mr = 0.92e-6;%0.16e-6 for 2 in parallel%0.109e-6 for 3 in
%parallel,0.081e-6 for 4,%0.06e-6 for 5% 0.054e-6for 6% 0.046e-6 for 7
%0.0408e-6 for 8% 0.0363e-6 for 9%  0.032e-6 for 10
```

```
% syms C_mr %= Ciss_2/5; cc. to juan rivas but this isnt true, Cmr
 sets the gain to 1
% assume(C_mr,{'positive','real'})
Q_c(1,n1) = 1./(ws.*Ciss_2(1,n1).*Rgd(1,n1));%linspace(5,200,100);
Q_mr = 50;
Q_f = 50;
R_mr_ws(1,n1) = (ws.*L_mr(1,n1))/Q_mr;
R_mr_3ws(1,n1) = (3*ws.*L_mr(1,n1))/Q_mr;
R_f_ws(1,n1) = (ws.*L_f(1,n1))/Q_f;
R_f_3ws(1,n1) = (3*ws.*L_f(1,n1))/Q_f;
R_f_tot_ws(1,n1) = R_f_ws(1,n1) + j*ws.*L_f(1,n1);
R_mr_tot_ws(1,n1) = R_mr_ws(1,n1) + j*ws.*L_mr(1,n1) +(1/
(j*ws.*C_mr(1,n1)));
R_f_tot_3ws(1,n1) = R_f_3ws(1,n1) + j*3*ws.*L_f(1,n1);
R_mr_tot_3ws(1,n1) = R_mr_3ws(1,n1) + j*3*ws.*L_mr(1,n1) +(1/
(j*3*ws.*C_mr(1,n1)));
Z_tank_tot_ws(1,n1) = (R_mr_tot_ws(1,n1).*R_f_tot_ws(1,n1))/
(R_mr_tot_ws(1,n1)+R_f_tot_ws(1,n1));
Z_tank_tot_3ws(1,n1) = (R_mr_tot_3ws(1,n1).*R_f_tot_3ws(1,n1))/
(R_mr_tot_3ws(1,n1)+R_f_tot_3ws(1,n1));
Z_ws(1,n1) = Z_tank_tot_ws(1,n1) + Rgd(1,n1) -(j/(ws.*Ciss_2(1,n1)));
Z_3ws(1,n1) = Z_tank_tot_3ws(1,n1) + Rgd(1,n1) -(j/
(3*ws.*Ciss_2(1,n1)));
% [n, d] = numden(simplify(Z_ws));
% [n3,d3] = numden(simplify(Z_3ws));
Abs_Z_ws(1,n1) = abs(Z_ws(1,n1));% %sqrt((real(n))^2+(imag(n))^2)/
sqrt((real(d))^2+(imag(d))^2);%
Abs_Z_3ws(1,n1) =abs(Z_3ws(1,n1));%  sqrt((real(n3))^2+(imag(n3))^2)/
sqrt((real(d3))^2+(imag(d3))^2);%
%vpasolve(Abs_Z_ws == (1/(ws*Ciss_2)))
%vpasolve(Abs_Z_ws == 3*Abs_Z_3ws);
%vpasolve(Abs_Z_3ws == (1/(3*ws*Ciss_2)))
% C_mr_final = ans%0.955e-9;1.911e-9 for 2 in parallel%2.86e-9 for 3
 in parallel, 3.8e-9 for 4
% L_mr_final = 1/(((ws*3)^2)*C_mr_final)%0.92e-6;%0.16e-6 for 2 in
 parallel%0.109e-6 for 3 in parallel, 0.081e-6 for 4
I_new(1,n1) = (sqrt(2)/3)*(Vg/pi).*((1./Abs_Z_ws(1,n1))+(1./
Abs_Z_3ws(1,n1)));
Rgd_loss_n(1,n1) = ((I_new(1,n1)).^2).*Rgd(1,n1);
I_f(1,n1) = I_new(1,n1).*abs(R_mr_tot_ws(1,n1))/
(abs(R_mr_tot_ws(1,n1)+R_f_tot_ws(1,n1)));
I_mr(1,n1) = I_new(1,n1).*(abs(R_f_tot_ws(1,n1))/
abs(R_mr_tot_ws(1,n1)+R_f_tot_ws(1,n1)));
I_f_ws(1,n1) = I_new(1,n1).*abs(R_mr_tot_ws(1,n1))/
(abs(R_mr_tot_ws(1,n1)+R_f_tot_ws(1,n1)));%(Vg/pi).*2*(1./Abs_Z_ws)
I_f_3ws(1,n1) = I_new(1,n1).*(abs(R_mr_tot_3ws(1,n1))/
abs(R_mr_tot_3ws(1,n1)+R_f_tot_3ws(1,n1)));%2*(Vg/pi).*(1./Abs_Z_3ws)
I_mr_ws(1,n1) = I_new(1,n1).*(abs(R_f_tot_ws(1,n1))/
abs(R_mr_tot_ws(1,n1)+R_f_tot_ws(1,n1)));%2*(Vg/pi).*(1./Abs_Z_ws)
I_mr_3ws(1,n1) = I_new(1,n1).* (abs(R_f_tot_3ws(1,n1))/
abs(R_mr_tot_3ws(1,n1)+R_f_tot_3ws(1,n1)));%2*(Vg/pi).*(1./Abs_Z_3ws)
Ind_loss(1,n1) =  0.5*((I_f_ws(1,n1).^2)*R_f_ws(1,n1)
 +(I_mr_ws(1,n1).^2)*R_mr_ws(1,n1) +
 (I_mr_3ws(1,n1).^2)*R_mr_3ws(1,n1)+(I_f_3ws(1,n1).^2)*R_f_3ws(1,n1));
```

```
% this is an assumption(I_f.^2).*R_f_ws + (I_mr.^2).*I_mr_ws1;
Sab_gate_drv_cond_n(1,n1) = (I_new(1,n1).^2)*R_sa;
Sub_gate_drv_sw = Cgs_sa*Vg_sa^2*fsw;
Ptot_gdrv_loss(1,n1) = Rgd_loss_n(1,n1) + Ind_loss(1,n1) +
 Sab_gate_drv_cond_n(1,n1) + Sub_gate_drv_sw;
Psw(1,n1) = Cgs_2_n(1,n1)*Vg^2*fsw;
PQW_vs_Phard(1,n1) = Ptot_gdrv_loss(1,n1)/Psw(1,n1);
Psoft_n(1,n1) = Ptot_gdrv_loss(1,n1);
Phard_n(1,n1) =  Psw(1,n1);
n1 = n1+1;
end
% figure
fplot(P_cond_total_2_per)
 plot(P_soft_hard);
 hold on
 plot(Ind_loss_n);
 plot(Rgd_loss_n);
 plot(Sab_gate_drv_cond_n);
 %plot(Phard_n);
 %plot(Psoft_n);
 hold off
 %plot(Q_c,PQW_vs_Phard);
 %ylabel('Psoft/Phard');
 legend('P-soft/P-hard','Ind loss','Rgd loss','Sadrv loss');
xlabel('n')
% %%Now we want to see if this EPC2023 is good with how many in
 parallel
%
% % Secondary total losses
P_FL = 50; %Each converter in parallel would be 50W contributed
Vin = 24; %Each converter is 24V
Vout = 1.8;
fsw = 3e6; %Frequency set is 3MHz
Ths = 1/(2*fsw);
D_FL = 0.45; % Full load at the maximum allowable phase shift ratio
N = 0.5*Vin/(Vout);
L_FL = ((1-D_FL)*D_FL*Ths*(N*Vout)^2)/(P_FL);
FOM_2 = 3.335e-12;  %3.335e-12 for epc2023
%Ron_2 = 1.45e-3;%linspace(0.1e-3,4e-3,100);% %1.45e-3 for epc2023 %
FOM_2 = 3.335e-12; %4e-12; %3.335e-12 for epc2023
Coss_2 =  2720e-12;% 2720e-12 for Si fet %2050e-12;for epc2023
Iout_FL = ((1-D_FL)*D_FL*Vin*N*Ths)/L_FL;
Iout_rms = Iout_FL / sqrt(2) ;
Vf = 1.2; %1.2V for Si fet %2V for epc2023;
k =1;
for k = 1:8
Coss_2 =  2720e-12*k; %2720e-12; %Si fet%2050e-12*k;
P_cond_sec(1,k) = 2*(Iout_rms)^2* Ron_2_n(1,k); % each converter is 4
 devices, 2 are conducting at a time
P_gate_sec(1,k) = 2*Psoft_n(1,k);
P_gate_hard_sec(1,k) = 2*Phard_n(1,k);
%P_sw_sec = 2*Coss_2*(Vout)^2*fsw
T_dead_sec(1,k) = (2*Vout*FOM_2/Iout_FL)./Ron_2_n(1,k);%at FL IL =
 55A, Tdead=0.75e-9 for epc2023
```

```
%P_dead_sec(1,k) = 2*Vf*Iout_FL*T_dead_sec(1,k)*fsw
P_total_sec_soft(1,k) = P_gate_sec(1,k) + P_cond_sec(1,k);
P_total_sec_hard(1,k) = P_gate_hard_sec(1,k) + P_cond_sec(1,k);
P_soft_vs_P_total_sec(1,k) = P_gate_sec(1,k)/P_total_sec_soft(1,k);
end
%figure
plot(P_total_sec_soft)
hold on
plot(P_total_sec_hard)
hold off
legend('Total soft gating','total hard gating');
ylabel('losses');
xlabel('number sw in parallel');
```

Total efficiency vs Load current

```
P_FL = 50; %Each converter in parallel would be 50W contributed
Vin = 24; %Each converter is 24V
Vout = 1.8;
fsw = 3e6; %Frequency set is 3MHz
Ths = 1/(2*fsw);
Vg = 5;
D_FL = 0.45; % Full load at the maximum allowable phase shift ratio
N = 0.5*Vin/(Vout);
L_main = ((1-D_FL)*D_FL*Ths*(N*Vout)^2)/(P_FL);
Ron_1 = 7e-3; %7mohms is the Ron of GS61008T
Coss_1 = 650e-12; %650pF is the Coss of GS61008T
Ciss_1 = 600e-12;%600pF is the Ciss of GS61008T
Vf_1 = 2; %GaN diode drop
I1_FL_pk = (Vin*0.5*D_FL*Ths)/(L_main);
Ron_2 = 0.55e-3; % One si device in sec
Coss_2 =  2720e-12;% 2720e-12 for Si fet %2050e-12;for epc2023
Iout_FL = ((1-D_FL)*D_FL*Vin*N*Ths)/L_main;
Iload = linspace(Iout_FL/100,Iout_FL,100);
Iload_rms = Iload./sqrt(2);
syms phi
e = [Iload == phi*(1-phi)*Ths*Vin*N/(L_main)];
p =1;
for p = 1:100
    inter = vpasolve(e(p));
    phi_load(p) = inter(1);
end
I1_load = (Vin*0.5*phi_load*Ths)/(L_main);
I1_rms = I1_load./sqrt(2);
P_cond_pri = I1_rms.^2*Ron_1;
P_gating_pri = Ciss_1*Vg^2*fsw;
P_pri = 2*(P_cond_pri+P_gating_pri);
P_cond_sec = 2*(Iload_rms).^2* Ron_2;
P_gating_sec = P_gate_sec(1);
P_sec = 2*(P_cond +P_gating_sec);
P_loss_total = P_pri+P_sec;
%From the total gating loss from the before section for (1) device
```

```
%Assuming both deadtime and switching losses in the primary and
 secndary
%are min by controls
Eff = 100./(100+P_loss_total);
figure
plot(P_loss_total)
hold on
plot(Eff)
hold off
legend('Total loss','total Sec loss');
ylabel('losses');
xlabel('% Iload');
%xticklabels(linspace(0.1,Iout_FL,100));
```

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Chapter 10

Appendix B

10.1 Resonant gate driver parameters Analysis Code

Half-Bridge multiresonant gate driver solution

```
fsw = 3e6;
Vg = 5;
Vg_sa = 5; %gating for GaN half brige
j = sqrt(-1);
ws = 2*pi*fsw;
Cgs_2_n = 7480e-12;%7480e-12; for Si FET %n1*(2050e-12) for spec2023;
Ciss_2 = 7700e-12;% 7700e-12;for Si FET %n1*2150e-12 for spec2023;
Rgd = 0.6;% 0.6;%(0.3)/n1;
Ron_2 = 0.55e-3;%0.55e-3 per Si FET
R_sa = 50e-3; %Driver Rout around 100mohms and below is better
 variation in soft and hard and soft gets more efficient
FOM_sa = 3.335e-12;
Cgs_sa = FOM_sa/R_sa;

syms C_mr positive real
syms L_f positive real
syms L_mr  positive real
% C_mr= Ciss_2*0.37;%2.52e-9;
%L_f =1/((ws^2)*Ciss_2);%0.4e-6;
%L_mr = 1/(((ws*3)^2)*C_mr);%0.22e-6;
Q_c = 1./(ws*Ciss_2.*Rgd);%linspace(5,200,100);
Q_mr = 50;
Q_f = 50;
R_mr_ws = (ws*L_mr)/Q_mr; %resistance in LMR at ws
R_mr_3ws = (3*ws*L_mr)/Q_mr;%resistance in LMR at 3ws
R_f_ws = (ws*L_f)/Q_f;%resistance in LF at ws
R_f_3ws = (3*ws*L_f)/Q_f;%resistance in LF at 3ws
Z_f_tot_ws = R_f_ws + j*ws*L_f; %Toal impedance in LF branch at ws
Z_mr_tot_ws = R_mr_ws + j*ws*L_mr +(1/(j*ws*C_mr));%Toal impedance in
 LMR branch
Z_f_tot_3ws = R_f_3ws + j*3*ws*L_f; %Toal impedance in LF branch at
 3ws
Z_mr_tot_3ws = R_mr_3ws + j*3*ws*L_mr +(1/(j*3*ws*C_mr));%Toal
 impedance in LMR branch at 3ws
Z_tank_tot_ws = (Z_mr_tot_ws*Z_f_tot_ws)/(Z_mr_tot_ws
+Z_f_tot_ws); %Toal impedance of resonant network at ws
Z_tank_tot_3ws = (Z_mr_tot_3ws*Z_f_tot_3ws)/(Z_mr_tot_3ws
+Z_f_tot_3ws);%Toal impedance of resonant network at 3ws
Z_ws = Z_tank_tot_ws + Rgd -(j/(ws*Ciss_2)); %Toal impedance including
 SW at ws
Z_3ws = Z_tank_tot_3ws + Rgd -(j/(3*ws*Ciss_2));%Toal impedance
 including SW at 3ws
[n, d] = numden(Z_ws);
[n3,d3] = numden(Z_3ws);

Abs_Z_ws = sqrt((real(n))^2+(imag(n))^2)/
sqrt((real(d))^2+(imag(d))^2); %Abs value at ws
Abs_Z_3ws = sqrt((real(n3))^2+(imag(n3))^2)/
sqrt((real(d3))^2+(imag(d3))^2);%Abs value at 3ws
```

```
eq1 = [solve(real(Z_ws)) == 0, solve(imag(Z_ws))>0]; % EQ1 => total
 impedance at ws should be inductive
eq2 = solve(abs(Z_ws)) == 3*solve(abs(Z_3ws)); %EQ2 => Gain at ws ==
 Gain at 3ws (Gain = 1/jw*C_iss /Z_ws)
eq3 = solve(angle(Z_ws))== solve(angle(Z_3ws)); % EQ3 => Phase at ws =
 Phase at 3ws
%eq4 = [solve(real(Z_3ws)) == 0, solve(imag(Z_3ws))>0] ;
eqns1 = [eq1,eq2,eq3];
vars1 = [C_mr,L_f,L_mr];
Y = vpasolve(eqns1,vars1);
C_mr_final = Y.C_mr
L_mr_final = Y.L_mr%1/(((ws*3)^2)*C_mr_final)
L_F_final = Y.L_f
```

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```
L=50e-9;
f1=3e6;
f2=2*f1;
f3=3*f1;
w1=2*pi*f1;
w2=2*w1;
w3=3*w1;
Z1=w1*L
Z2=w2*L
Z3=w3*L
Cb=0.030e-6;
ZC1=-1/w1/Cb
ZC2=-1/w2/Cb
ZC3=-1/w3/Cb
Lm=13.8e-6;
Zm1=w1*Lm
Zm2=w2*Lm
Zm3=w3*Lm
Ciss=7.7e-9;
ZCiss=-1/w1/Ciss
Zeq=Zm1*ZCiss/(Zm1+ZCiss)
Lk = 48e-9;
Z1 = w1*Lk - 1/(w1*Cb) - 1/(w1*Ciss)
Z3 = Zm1*Z1/(Zm1+Z1)
Z4 = Z3 - 1/(w1*Cb) + w1*Lk
Ceq = -1/(w1*Z4)
Cres1 = Ceq+Ciss
Lf = 1/(2*Cres1*(w1^2))
Lmr = 500e-9;
Cmr = -1/((w2^2)*Lmr)
```

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Chapter 11

Appendix C

11.1 Dual Active Bridge Converter Schematic

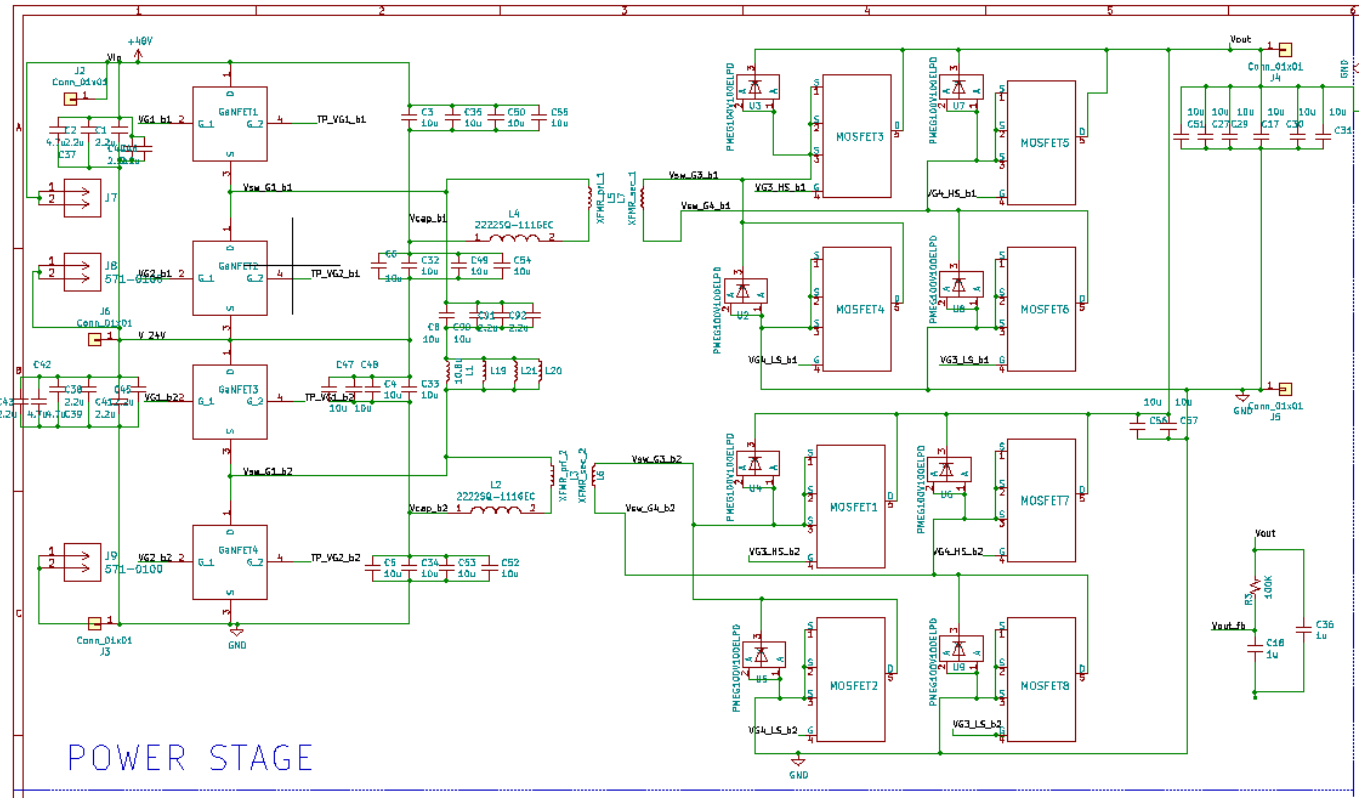

Figure 11.1: Power Stage KiCAD Schematic

11.2 Gate Driver Schematic

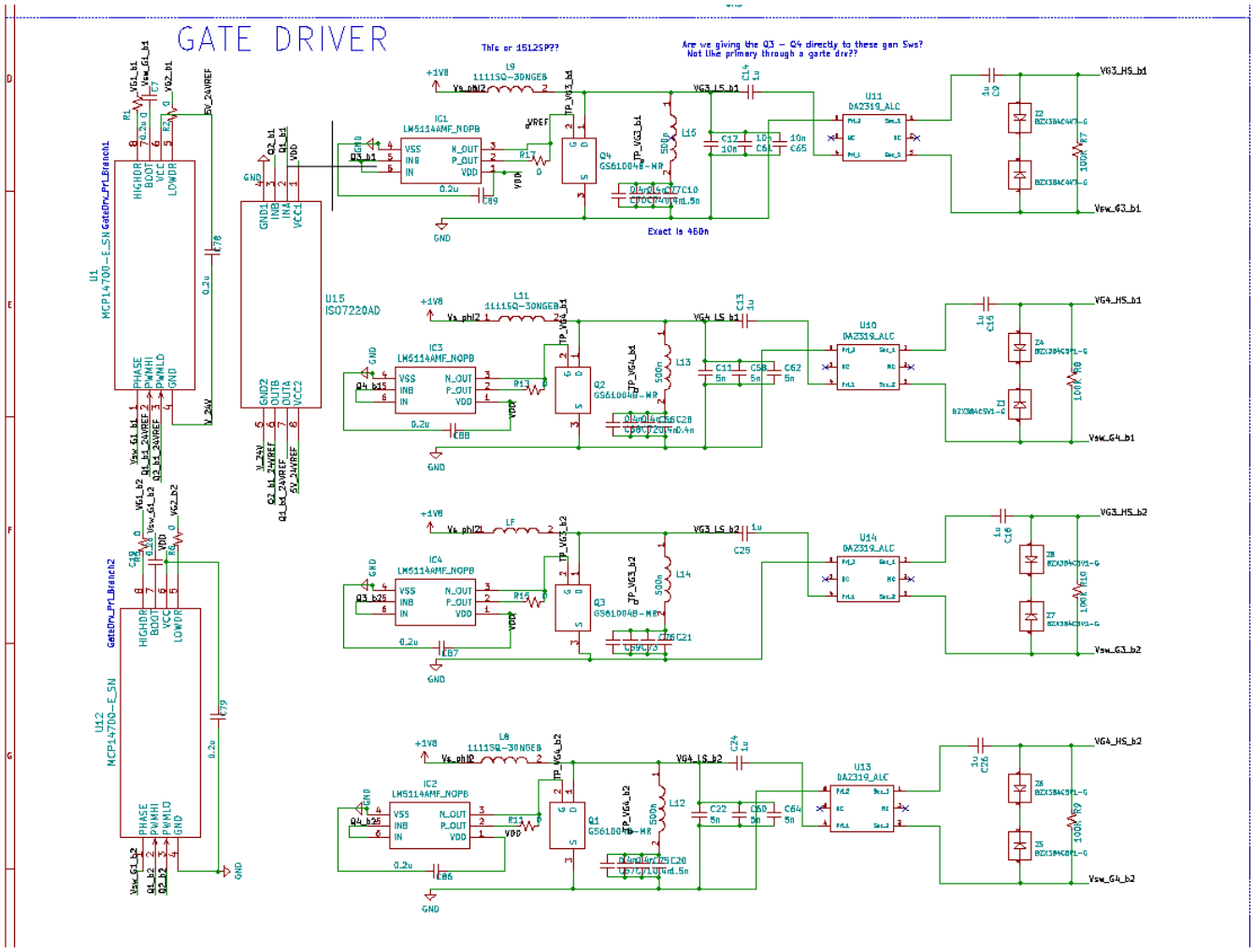

Figure 11.2: Gate Driver Stage KiCAD Schematic

11.3 Peripherals Schematic

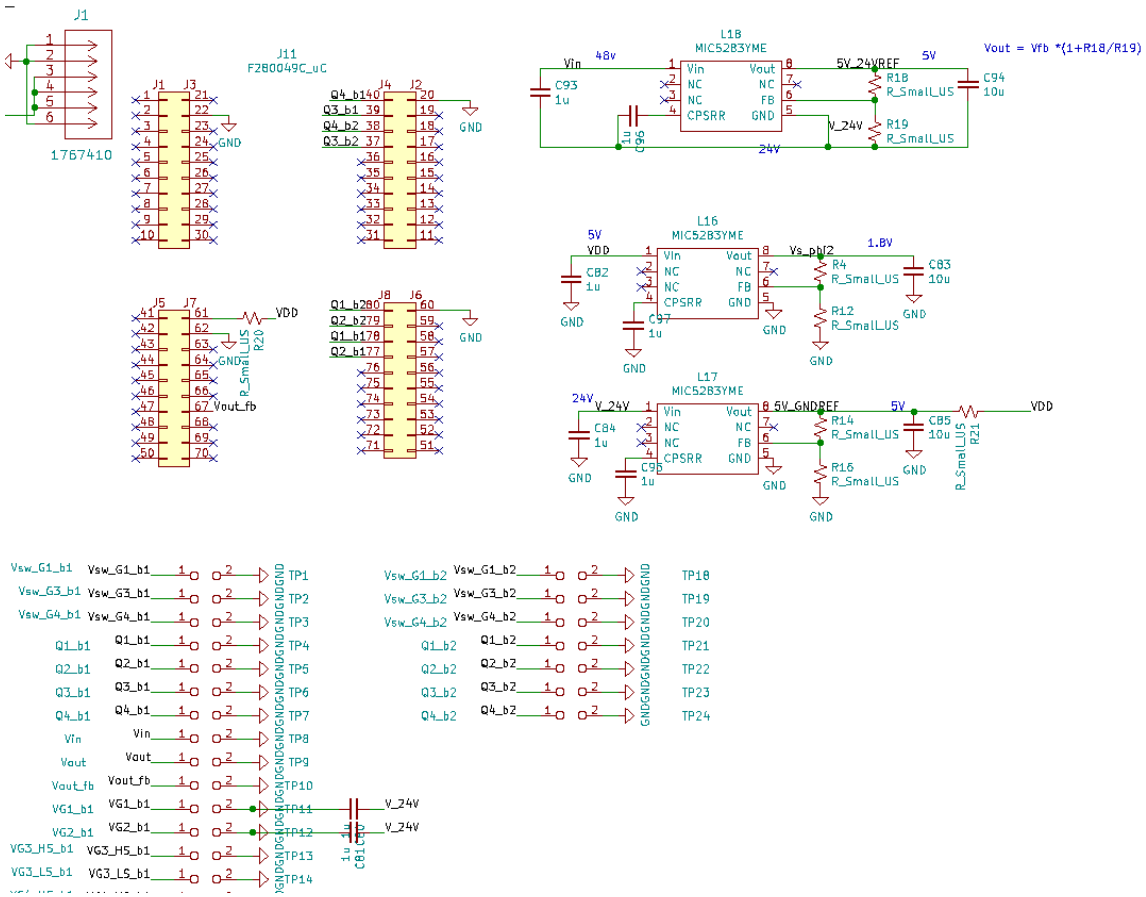

Figure 11.3: Peripherals and Gate Driver power supplies KiCAD Schematic

Chapter 12

Appendix D

12.1 Dual Active Bridge converter Layout

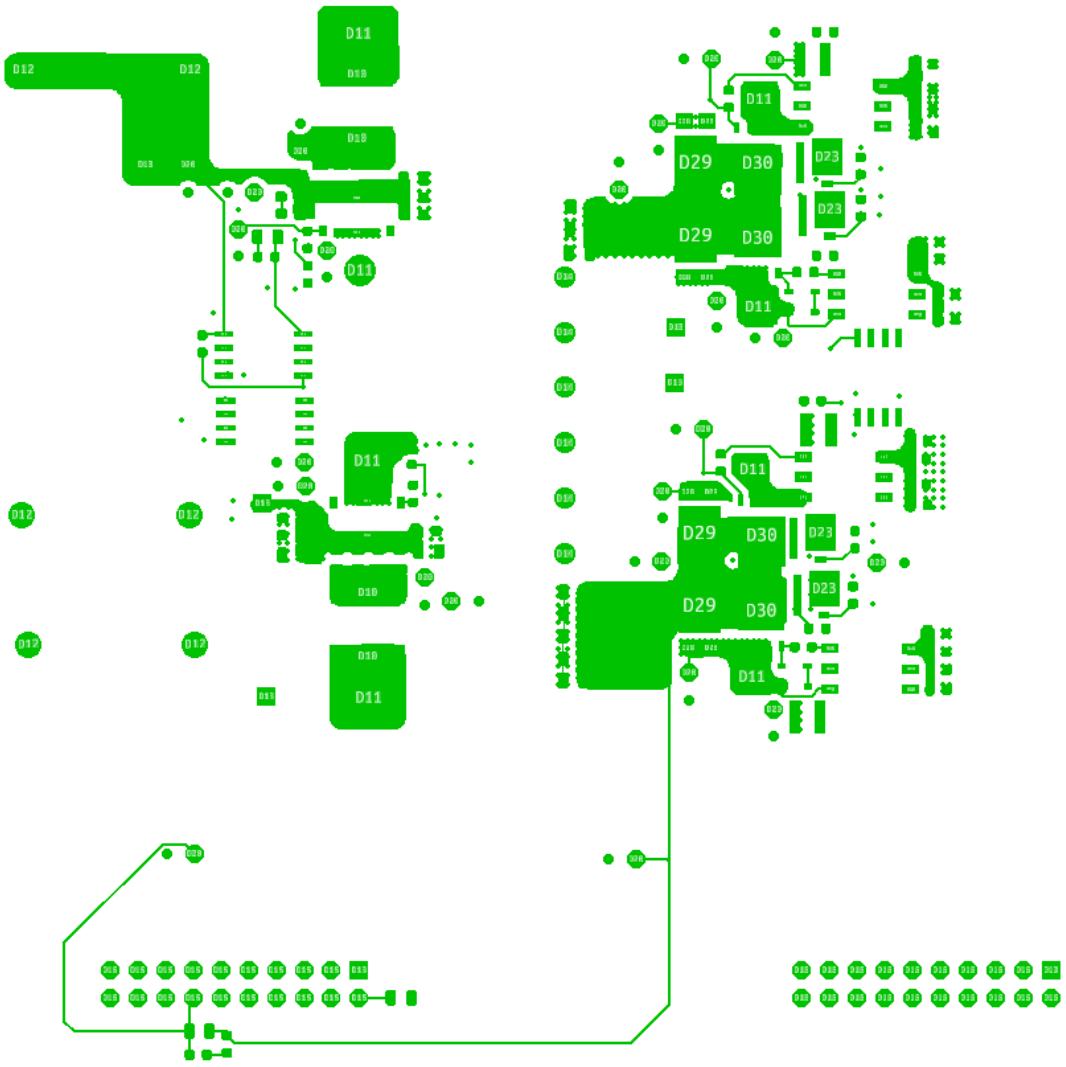

Figure 12.1: Layout First layer

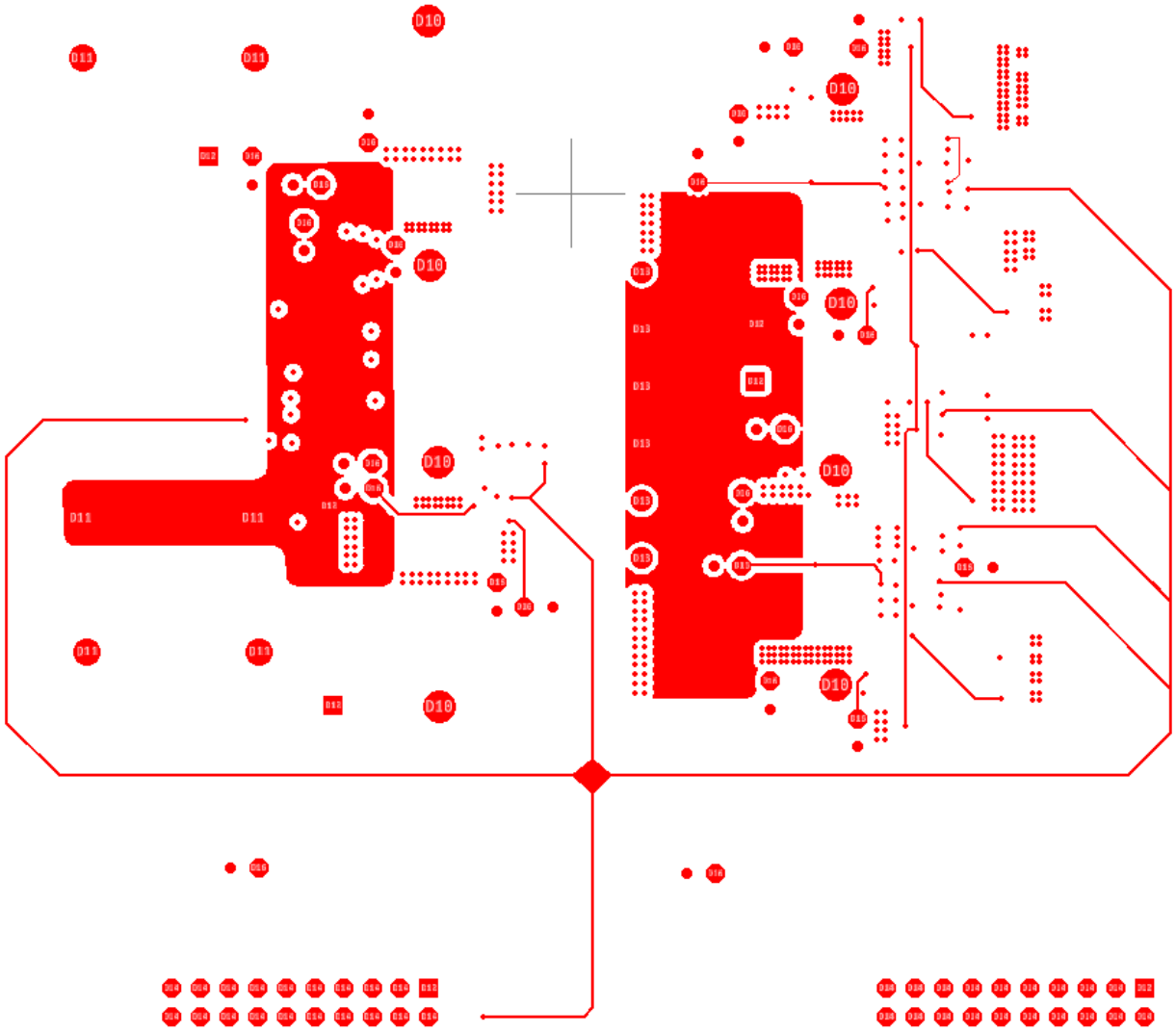

Figure 12.2: Layout second layer

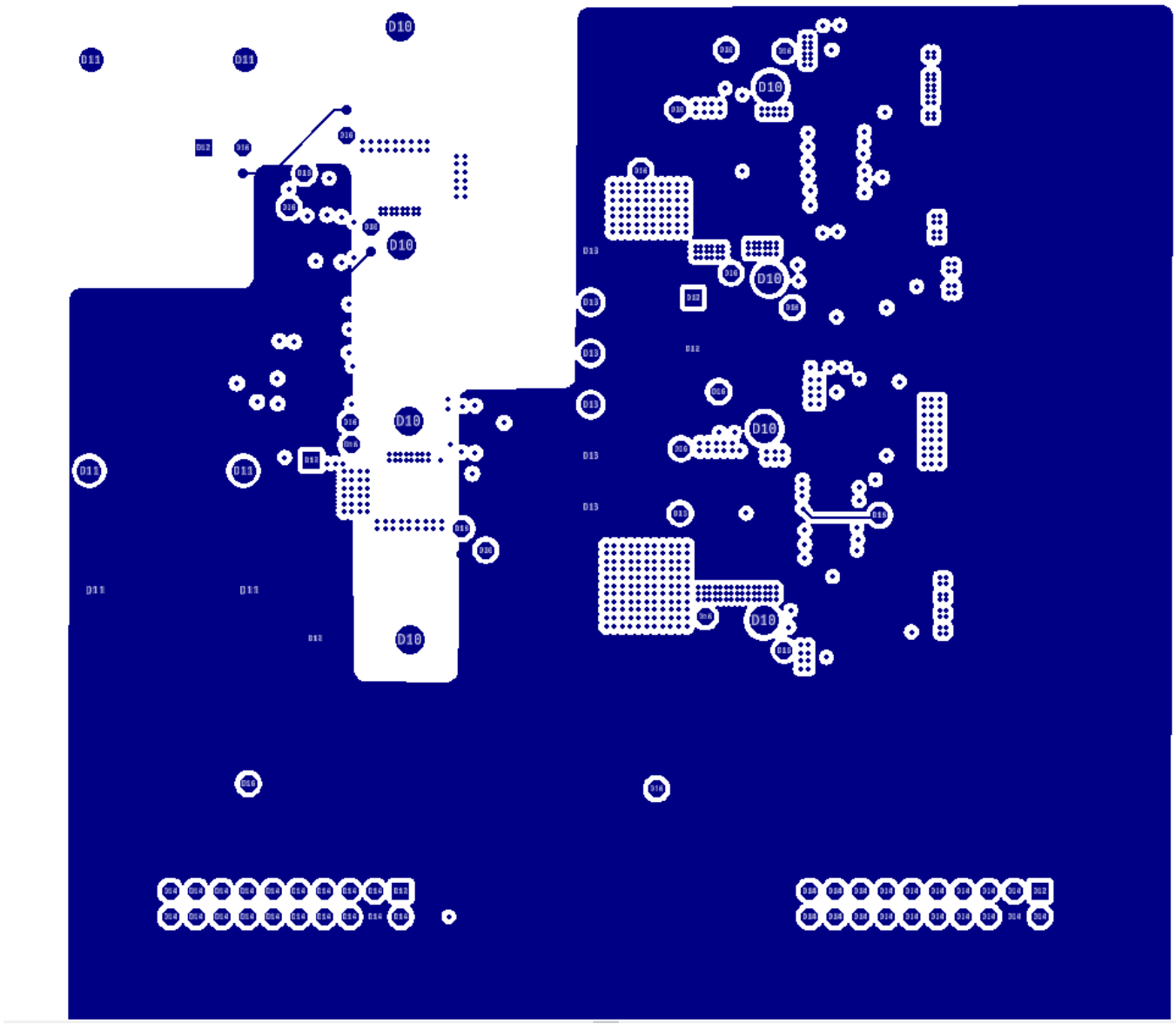

Figure 12.3: Layout Third layer

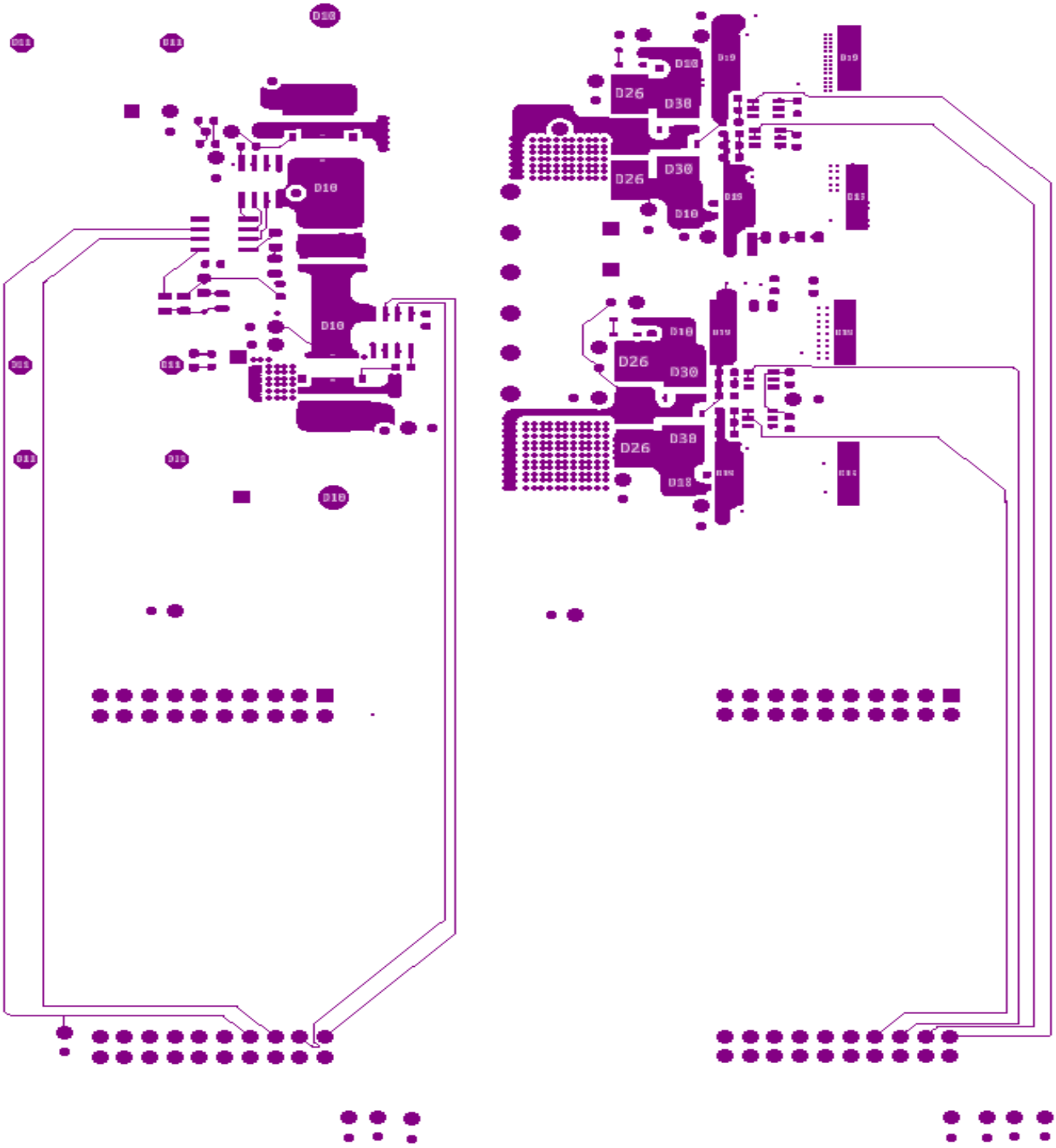

Figure 12.4: Layout Fourth layer

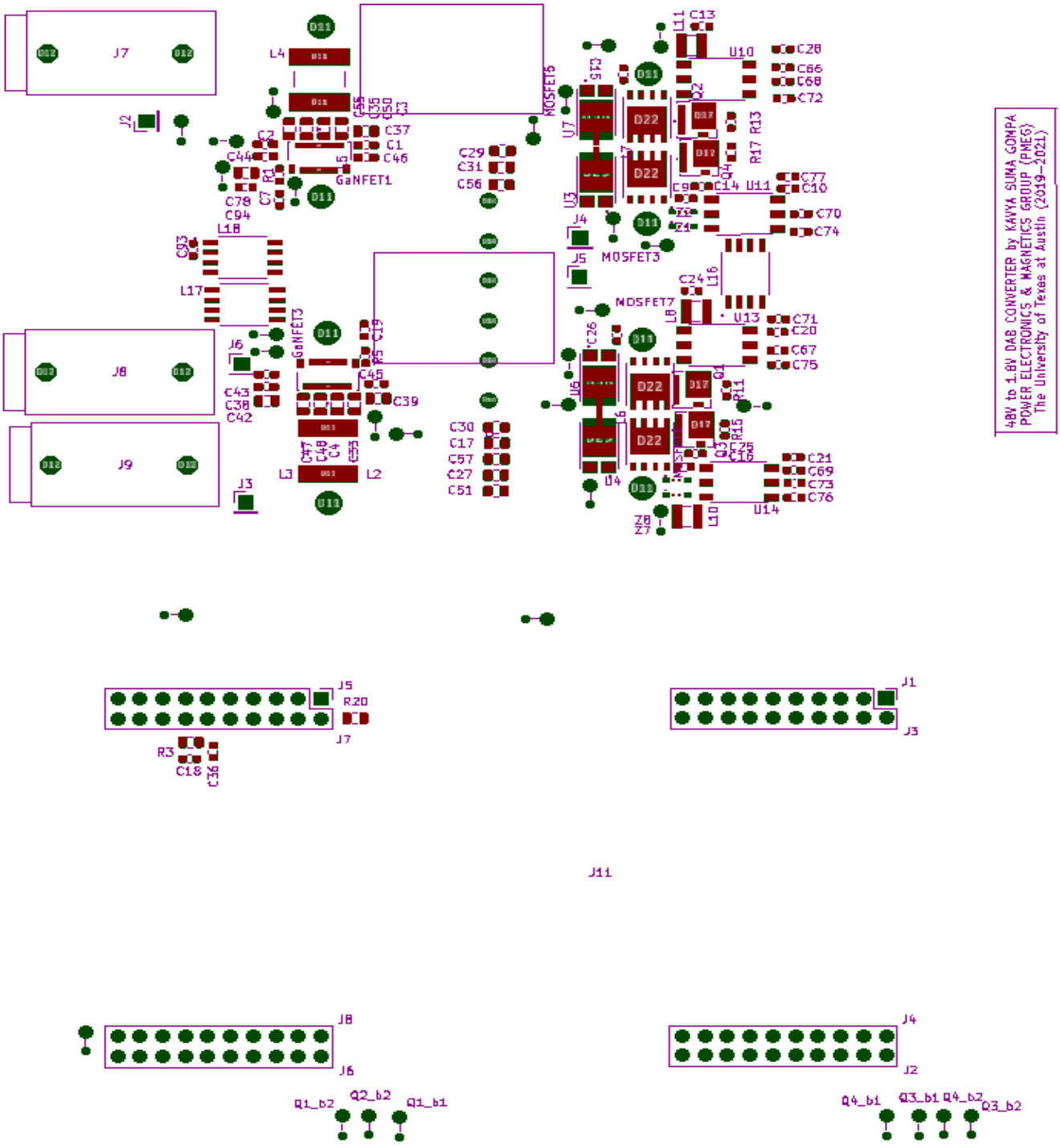

Figure 12.5: Layout Top mask and silk layer

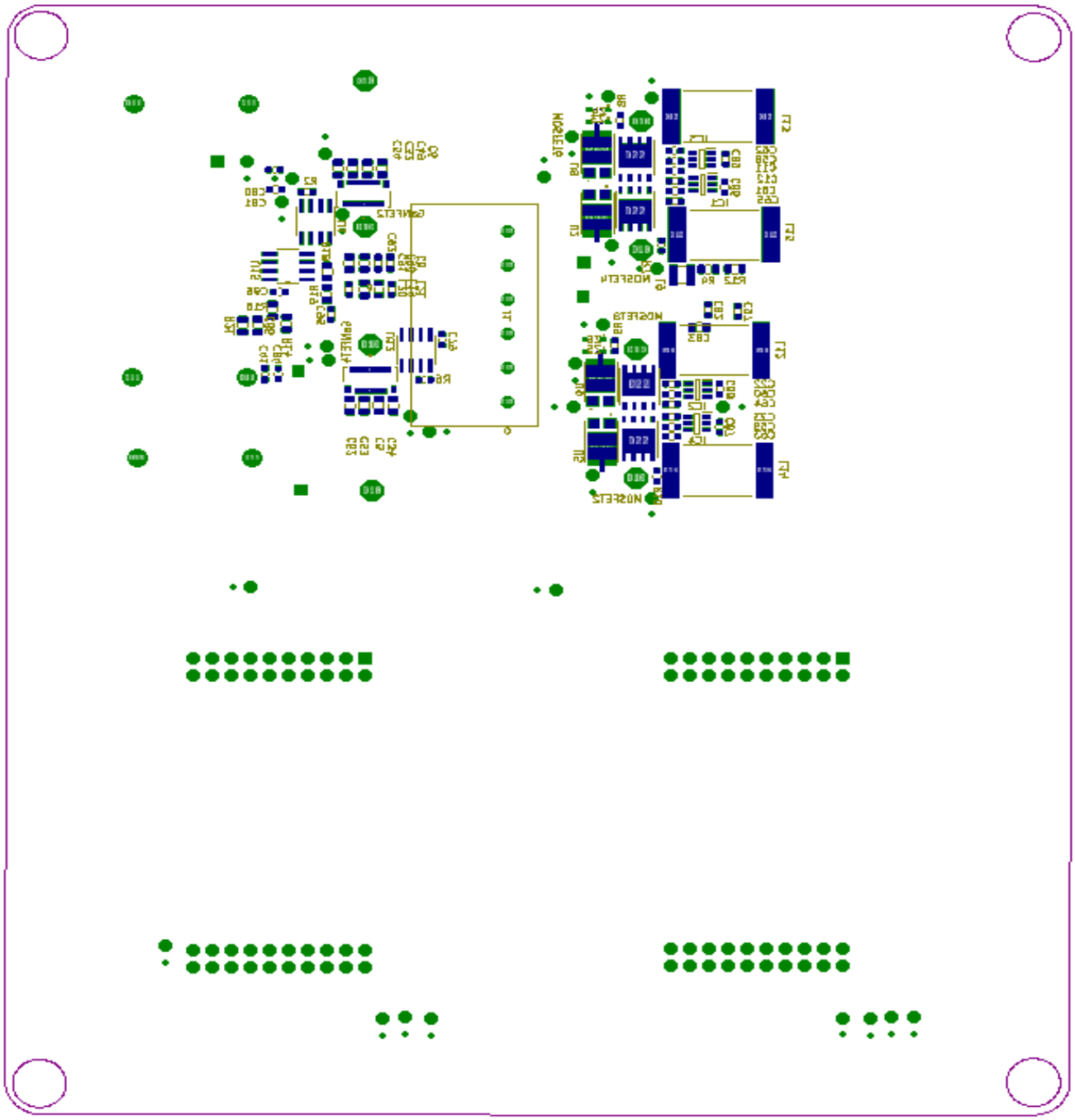

Figure 12.6: Layout bottom mask and silk layer

Bibliography

[1] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, 2014.

[2] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800–2810, 2012.

[3] X. Fei, Z. Feng, N. PuQi, and W. Xuhui, "Analyzing ZVS Soft Switching Using Single Phase Shift Control Strategy of Dual Active Bridge Isolated DC-DC Converters," in *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, pp. 2378–2381, 2018.

[4] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, 1991.

[5] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Transactions on Electron Devices*, vol. 36, no. 9, pp. 1811–1823, 1989.

[6] T. McDonald, "GaN Based Power Technology Stimulates Revolution in Power Conversion Electronics," *Electronics in Motion and Conversion*, pp. 2–4, 2009.

[7] G. H. Aghdam, "Model characterization and performance evaluation of GaN FET in DC-DC POL regulators," in *2015 IEEE International Telecommunications Energy Conference (INTELEC)*, pp. 1–4, 2015.

[8] C. C. Mi, H. Bai and S.Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional dc-dc converter," *IET Power Electron*, vol. 1, no. 4, pp. 507–517, 2008.

[9] A. R. Rodríguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 1129–1135, 2010.

[10] G. G. Oggier, M. Ordonez, J. M. Galvez, and F. Luchino, "Fast Transient Boundary Control and Steady-State Operation of the Dual Active Bridge Converter Using the Natural Switching Surface," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 946–957, 2014.

[11] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, 2014.

[12] B. Zhao, Q. Yu, and W. Sun, "Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4667–4680, 2012.

[13] A. R. Rodríguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 1129–1135, 2010.

[14] A. R. Rodríguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 1129–1135, 2010.

[15] Y. Jang and M. Jovanovic, "A new family of full-bridge zvs converters," in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03.*, vol. 2, pp. 622–628 vol.2, 2003.

[16] J. Li, Z. Chen, Z. Shen, P. Mattavelli, J. Liu, and D. Boroyevich, "An adaptive dead-time control scheme for high-switching-frequency dual-active-bridge converter," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1355–1361, 2012.

[17] A. Pizzutelli, A. Carrera, M. Ghioni, and S. Saggini, "Digital dead time auto-tuning for maximum efficiency operation of isolated dc-dc converters," in *2007 IEEE Power Electronics Specialists Conference*, pp. 839–845, 2007.

[18] K. Takagi and H. Fujita, "Dynamic control and dead-time compensation method of an isolated dual-active-bridge DC-DC converter," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–10, 2015.

[19] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, vol. 2, pp. 911–917 Vol. 2, 2005.

[20] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *2006 37th IEEE Power Electronics Specialists Conference*, pp. 1–7, 2006.

[21] D. Aggeler in *Power Conversion Conference - Nagoya, title=Bi-Directional Isolated DC-DC Converter for Next-Generation Power Distribution - Comparison of Converters using Si and SiC Devices*, pp. 510–517, 2007.

[22] H. Bai, C. C. Mi, and S. Gargies *IEEE Transactions on Power Electronics, title=The Short-Time-Scale Transient Processes in High-Voltage and High-Power Isolated Bidirectional DC–DC Converters*, vol. 23, no. 6, pp. 2648–2656, 2008.

[23] D. Maksimovic, "A MOS gate drive with resonant transitions," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, pp. 527–532, 1991.

[24] Yuhui Chen, F. C. Lee, L. Amoroso, and Ho-Pu Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 470–477, 2004.

[25] L. Gu, Z. Tong, W. Liang, and J. Rivas-Davila, "A Multiresonant Gate Driver for High-Frequency Resonant Converters," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 1405–1414, 2020.

[26] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very-High-Frequency Resonant Boost Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1654–1665, 2009.

[27] M. P. Madsen, J. A. Pedersen, A. Knott, and M. A. E. Andersen, "Self-oscillating resonant gate drive for resonant inverters and rectifiers composed solely of passive components," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 2029–2035, 2014.

[28] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," in *2006 37th IEEE Power Electronics Specialists Conference*, pp. 1–11, 2006.

[29] H. Jedi, M. K. Kazimierczuk, and A. Reatti, "A Current-Source Sinusoidal Gate Driver for High-Frequency Applications," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2018.

[30] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very High Frequency Resonant Boost Converters," in *2007 IEEE Power Electronics Specialists Conference*, pp. 2718–2724, 2007.

[31] H. Jedi, T. Salvatierra, A. Ayachit, and M. K. Kazimierczuk, "High-Frequency Single-Switch ZVS Gate Driver Based on a Class Φ_2 Resonant Inverter," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4527–4535, 2020.

[32] Z. Kaczmarczyk, "High-Efficiency Class E,$hboxEF_2$, and$hboxE/F_3$Inverters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1584–1593, 2006.

[33] H. Jedi, "Resonant gate-drive circuits for high-frequency power converters," 2018.

[34] J. Rivas, *Radio frequency dc-dc power conversion.* PhD thesis, Massachusetts Institute of Technology, 2006.

[35] R. S. Yang, A. J. Hanson, D. J. Perreault, and C. R. Sullivan, "A low-loss inductor structure and design guidelines for high-frequency applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 579–586, 2018.

[36] A. J. Hanson, J. A. Belk, S. Lim, C. R. Sullivan, and D. J. Perreault, "Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7909–7925, 2016.

[37] K. Xu, C. Fu, Y. Wang, and H. Wang, "Voltage and current balance control for the isop converter-based power electronic transformer," in *2015 18th International Conference on Electrical Machines and Systems (ICEMS)*, pp. 378–382, 2015.

[38] G. Xu, D. Sha, and X. Liao, "Decentralized inverse-droop control for input-series–output-parallel dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4621–4625, 2015.

[39] J. Shi, J. Luo, and X. He, "Common-duty-ratio control of input-series output-parallel connected phase-shift full-bridge dc–dc converter modules," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3318–3329, 2011.

[40] D. Sha, Z. Guo, and X. Liao, "Cross-feedback output-current-sharing control for input-series-output-parallel modular dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2762–2771, 2010.

[41] D. Sha, Z. Guo, T. Luo, and X. Liao, "A general control strategy for input-series–output-series modular dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3766–3775, 2014.

[42] Q. Wei, B. Wu, D. Xu, and N. R. Zargari, "Model predictive control of capacitor voltage balancing for cascaded modular dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 752–761, 2017.

[43] L. Qu, D. Zhang, and Z. Bao, "Output current-differential control scheme for input-series–output-parallel-connected modular dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5699–5711, 2017.

[44] L. Qu, D. Zhang, and B. Zhang, "Input voltage sharing control scheme for input series and output parallel connected dc–dc converters based on peak current control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 429–439, 2019.

[45] M. Abrehdari and M. Sarvi, "Comprehensive sharing control strategy for input-series output-parallel connected modular dc–dc converters," *IET Power Electronics*, vol. 12, no. 12, pp. 3105–3117.

[46] X. Ruan, W. Chen, L. Cheng, C. K. Tse, H. Yan, and T. Zhang, "Control strategy for input-series–output-parallel converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 4, pp. 1174–1185, 2009.

[47] F. Deng, X. Zhang, X. Li, T. Lei, and T. Wang, "Decoupling control strategy for input-series output-parallel systems based on dual active bridge dc-dc converters," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–8, 2018.

[48] S. Sanders, J. Noworolski, X. Liu, and G. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251–259, 1991.

[49] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2078–2084, 2012.

[50] V. Caliskan, O. Verghese, and A. Stankovic, "Multifrequency averaging of dc/dc converters," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 124–133, 1999.

[51] C. Basso, *Designing Control Loops for Linear and Switching Power Supplies Power Supplies: A Tutorial Guide*. 2012.

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